CONFIDENTIAL B

MT6755 Design Notice V1.6

2016/06

MT6755 Design Notice Versions

- MT6755 baseband design notice

Category	Description	Date	Version	Remark
BB	BB design notice	2016/06/24	V1.6	
BB	SD & eMMC design note	NA	NA	Common
BB	Camera design notice	NA	NA	Common
BB	USB design notice	NA	NA	Common
BB	LCM design notice	NA	NA	Common
BB	SIM design notice	NA	NA	Common
BB	Capacitive type touch panel design notice	NA	NA	Common
BB	G/M/ALS & PS/pressure sensor design notice	NA	NA	Common
BB	ESD design notice	NA	NA	Common
BB	Memory design notice	NA	NA	Common
BB	MHL (DPI) design notice	NA	NA	Common
BB	eFuse design notice	NA	NA	Common

MT6755 Design Notice Version History

- MT6755 turnkey solution design notice

Category	Description
MT6755	MT6755 design notice
	PCB layout/PDN/MMD/SMT guide
	SCH and PCB design checklist
PMIC (MT6351)	MT6351 PMIC design notice
	MT6311 PMIC design notice
	Charger design notice
	Battery selection guideline
	MT6351 audio & speech design notice
	MT6351 RTC design notice
Connectivity (MT6625L/MT6630)	MT6625L design notice
	MT6630Q combo chip design notice
RF (MT6176)	MT6176 design notice
Common	Thermal design notice
	LTE phone ANT guideline
	MT6605 design notice

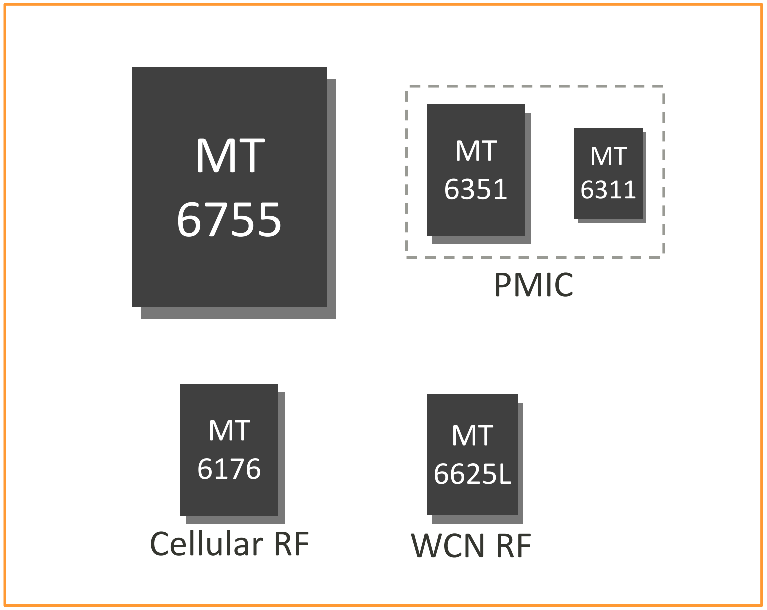
Find the turnkey solution design notices on DCC.

Change List (1)

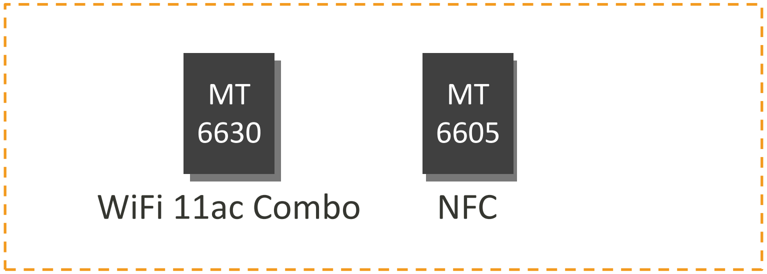
Version	Date	Description
V0.1	2015.04.27	1. 1st release
V0.2	2015.06.30	1. Update Apps CPU & Graphic spec. (page 6) 2. Add usage description for RAMDUMP - External Key (page 14) 3. Add DSI_TE notice description (page 48-49) 4. Add SSUSB P/N swap description for USB (page 68) 5. Update IDDIG description for USB (page 69) 6. Add MHL design notice (page 78)
V1.0	2015.08.28	1. Update USB IDDIG description for USB (page 69) 2. Update IRTX connection (page 72) 3. Update JTAG trapping description and need to add external 4.7k pull-up resistor (page 87)
V1.1	2015.11.05	1. Update Apps CPU, Memory & Graphic spec. (page 6) 2. Update Front (sub) Camera description (page 62)
V1.2	2016.02.15	1. Add SIM Schematic Notice: Without NFC Application (page 43) 2. Add SPI0 notice for fingerprint sensor security application (page 87)
V1.3	2016.03.10	1. Add PWM_A/B/C for IR_TX (page 74 & 78) 2. Modify EINTs application note(Page 24)
V1.4	2016.03.18	1. Modify PWM application note(Page 85) 2. Add SPI1 not support TEE SPI for security application(Page 87)
V1.5	2016.05.06	1. Add" Select N.C. on Def. Mode for UNUSED PIN, otherwise you may encounter unexpected issue due to wrong setting. "(Page18)
V1.6	2016.06.24	1. Modify VMC&VMCH voltage description, Sync with software settings(Page13) 2. Modify Pull up description of GPIO42(Page71)

Baseband Design Notice

MT6755 Platform Chipset



MT6755 platform		Package size	Type	Pitch	Pin #
BB	MT6755	13.0 x 13.4 x 0.9	TFBGA	0.4	873
RF	MT6176	6.2 x 6.2 x 0.9	aS3	0.4	196
WCN	MT6625L	5.0 x 5.0 x 0.85	QFN40	0.4	40
PMIC	MT6351	7.0 x 7.0 x 0.9	FCCSP	0.4	199
PMIC	MT6311	2.2 x 2.6 x 0.53	WLCSP	0.4	30



Optional Chips		Package size	Type	Pitch	Pin #
WCN	MT6630	5.0 x 5.0 x 0.53	WLCSP	0.4	113
WCN	MT6605	4.0 x 4.0 x 0.85	QFN	0.4	32

MT6755 High-Level Spec Comparisons

	MT6752	MT6755
Process	28HPM	28HPM
Apps CPU	8x Cortex-A53, up to 1.7GHz	4x Cortex-A53, **1.95GHz** + 4x Cortex-A53, **1.15GHz**
Memory	1x LPDDR3 800MHz (LPDDR3-1600) up to 3GB eMMC 5.0	1x LPDDR3 **833.5MHz (LPDDR3-1667)** up to **4GB** eMMC **5.1**
Camera	16MP @ 30fps w/ ZSD Dual ISP	**21MP @ 24fps** / 16MP @ 30fps w/ ZSD Dual ISP w/ **improved 3A/denoise/demosaic/sharpness**
Video decoding	1080p 30fps H.264/265	1080p 30fps H.264/265 w/ **25% power improvement**
Video encoding	1080p 30fps H.264	1080p 30fps H.264 w/ **25% power improvement**
Graphics	ARM Mali-T760 MP2 700MHz	ARM **Mali-T860** MP2 **728MHz**
Display	FHD 1920x1080 w/ 8 Blending Layer	FHD 1920x1080 w/ **12** Blending Layer
Modem	LTE FDD/TDD R9 Cat4 (150/50Mbps) DC-HSPA+, TD-SCDMA, EDGE	LTE FDD/TDD R11 **Cat-6 with 2x20 CA (300/50Mbps)** DC-HSPA+, TD-SCDMA, EDGE **CDMA2000 1x/EVDO Rev. A (3.1/1.8Mbps, SRLTE)** **LTE/GPS Co-clock Supported**
RF	Single RF for LTE/WCDMA/TD/EDGE 8/8 Primary/Diversity RX Ports	Single RF for **LTE 2x20 CA**/WCDMA/TD/EDGE/**C2K** **14/14** Primary/Diversity RX Ports
Connectivity	Wi-Fi abgn w/ throughput up to 78Mbps GPS/Glonass/Beidou, BT/FM	Wi-Fi abgn w/ **throughput up to 90Mbps** GPS/Glonass/Beidou w/ **improved TTFF & Drift,** BT/FM

Peripherals Comparisons

	MT6752	MT6755
USB	USB 2.0 & IC-USB	USB 2.0/USB **3.0** & IC-USB
SDIO	3 (1 for VIA C2K modem)	2
SPI	1	**2**
PWM	3	3
UART	4	2 (AP/modem logging shared; MT6630/DSDA shared)
Consumer IR	Not supported	**Supported (TX only)**
I2C	4 (1 for MT6311)	5 (1 for MT6311)
I2S	4	4
Audio AMP	Integrated	Not Integrated (requires ext. solution)
AUXADC	1 ADC with 3-channel inputs	1 ADC with **5**-channel inputs
PCM	2	2
GPIO	187	**190**

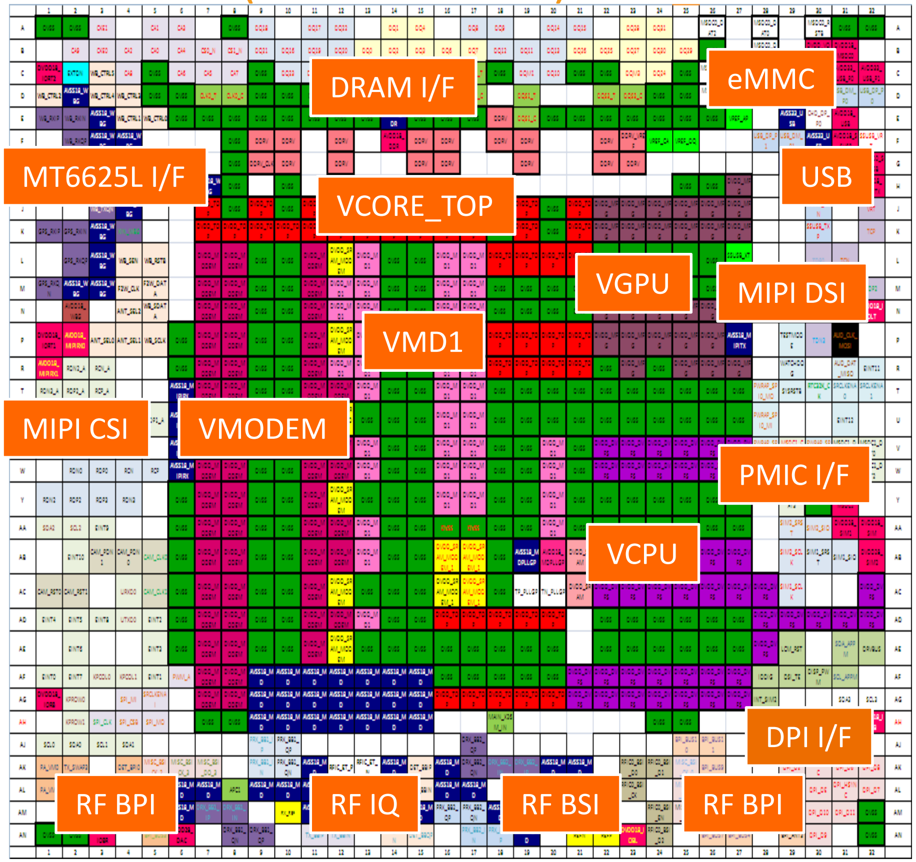
Ball Map

MT6755 Ball Map

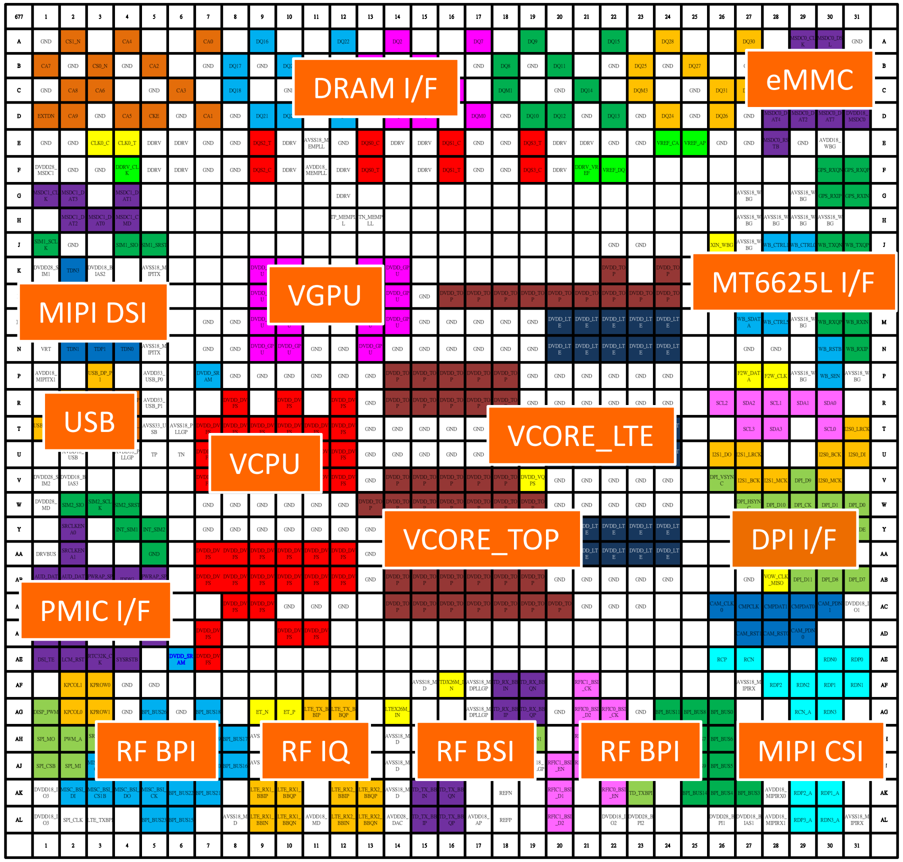
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
A	DVSS	DVSS	CKE1		CA1	CA3		DVSS	DQ16		DQ17	DQ22		DQ1	DQ4		DQ8	DQ9		DQ14	DQ15		DQ28	DQ31		MSDC0_DAT2		MSDC0_DAT0		MSDC0_RSTB	DVSS	DVSS	A
B		CA9	CKE0	CA2	CA0	CA4	CS0_N	CS1_N	DQ21	DQ18	DQ19	DQ20	DQ0	DQ2	DQ3	DQ6	DQ7	DQ12	DQ11	DQ13	DQ26	DQ25	DQ27	DQ30	DQ29	DVSS		MSDC0_DAT3		DVDD_VQPS	DVDD18_MSDC0		B
C	DVDD18_IORT2	EXTCON	WB_CTRL5	CA8	DVSS	CA6	CA5	CA7	DVSS	DQ23	DQM2	DVSS	DVSS	DVSS	DQ5	DQM0	DQS0_T	DVSS	DQM1	DQ10	DVSS	DVSS	DQM3	DQ24	DVSS	MSDC0_DAT4	MSDC0_DAT1	MSDC0_DAT5	MSDC0_DAT6	MSDC0_DAT7	AVDD33_USB_P0	AVDD33_USB_P1	C
D	WB_CTRL3	AVSS18_WBG	WB_CTRL4	WB_CTRL2	DVSS	DVSS	CLK0_T	CLK0_C	DVSS	DVSS	DVSS	DQS2_T	DQS2_C	DVSS	DVSS	DVSS	DQS0_C		DQS1_T			DQS3_T	DQS3_C	DVSS	DVSS	MSDC0_CMD	MSDC0_DSL	MSDC0_CLK		CHD_DM_P0	USB_DM_P0	USB_DP_P0	D
E	WB_RXIP	WB_RXIN	AVSS18_WBG	WB_CTRL1	WB_CTRL0	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	AVSS18_DDR	DVSS	DVSS	DVSS	DDRV	DQS1_C	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VREF_AP		AVSS33_USB	CHD_DP_P0	AVDD18_USB		E
F		WB_RXQP	AVSS18_WBG	AVSS18_WBG				DVSS	DDRV	DDRV		DDRV		AVDD18_DDR	DDRV	DDRV		DDRV	DDRV			DDRV	DDRV_VREF	VREF_CA	VREF_DQ			USB_DP_P1	USB_DM_P1	AVSS33_USB	AVDD18_SSUSB	SSUSB_VRT	F
G	WB_TXIP	WB_RXQN	AVSS18_WBG	AVSS18_WBG				DVSS	DDRV_CLK	DDRV		DDRV			DDRV	DDRV			DDRV			DDRV	DDRV						AVSS33_USB	SSUSB_RXN	SSUSB_RXP	AVDD33_SSUSB	G
H	WB_TXIN	WB_TXQP	AVSS18_WBG	AVSS18_WBG			AVSS18_WBG	DVSS		DVSS					TP_MEMPLL	TN_MEMPLL									DVSS	DVSS	DVDD_MFG			AVSS10_SSUSB	AVSS18_MIPITX	AVDD18_MIPITX	H
J			WB_TXQN	AVSS18_WBG			DVDD_TOP	DVSS	DVDD_TOP	DVSS	DVDD_TOP		DVSS	DVSS			DVDD_TOP	DVSS	DVDD_TOP	DVSS	DVDD_TOP	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG			SSUSB_TXN		VRT	J
K	GPS_RXIP	GPS_RXIN	AVSS18_WBG	XIN_WBG			DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVSS	DVDD_TOP	DVSS	DVDD_TOP	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG			SSUSB_TXP		TCP	K
L		GPS_RXQP	AVSS18_WBG	WB_SEN	WB_RSTB		DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_SRAM_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVSS	DVSS	DVSS	DVSS	DVSS	SSUSB_XTALI			TDP0	TCN		L
M	GPS_RXQN	AVSS18_WBG	AVSS18_WBG	F2W_CLK	F2W_DATA		DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS			TDP1	TDN0	TDN2	TDP2	M
N		AVDD18_WBG		ANT_SEL2	WB_SDATA		DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG			TDN1	TDP3	AUD_DAT_MOSI	DVDD18_IOLT	N
P	DVDD18_IORT1	AVDD18_MIPIRX0	ANT_SEL0	ANT_SEL1	WB_SCLK	DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_SRAM_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	DVDD_MFG	AVSS18_MIPITX		TESTMODE	TDN3	AUD_CLK_MOSI		P
R	AVDD18_MIPIRX1	RDN2_A	RCN_A			DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVSS	DVDD_MFG	DVSS	DVDD_MFG	DVDD_MFG	DVDD_MFG		WATCHDOG		AUD_DAT_MISO	EINT11	R
T	RDN3_A	RDP2_A	RCP_A			AVSS18_MIPIRX	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	PWRAP_SPI0_MO	SYSRSTB	RTC32K_CK	SRCLKENA0	SRCLKENA1	T
U	RDP3_A	RDN0_A	RDP0_A	RDN1_A	RDP1_A	AVSS18_MIPIRX	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_SRAM_MODEM	DVSS	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	PWRAP_SPI0_MI			EINT12		U
V	RDP1	RDN1				AVSS18_MIPIRX		DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVSS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	PWRAP_SPI0_CSN	MSDC1_CLK	PWRAP_SPI0_CK	MSDC1_DAT1	MSDC1_DAT0	V
W		RDN0	RDP0	RCN	RCP	AVSS18_MIPIRX	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVSS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS		MSDC1_CMD		DVDD28_MC1	MSDC1_DAT2	W
Y	RDN2	RDP2	RDP3	RDN3		DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_SRAM_MODEM	DVSS	DVSS	DVSS	DVDD_MD1	DVDD_MD1	DVSS	DVSS	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		MSDC1_DAT3	DVSS	DVDD28_MSDC1		Y
AA	SDA2	SCL2	EINT9			DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MODEM	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_MD1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		SIM2_SRST	SIM2_SIO	DVDD28_SIM1	DVDD18_SIM	AA
AB		EINT10	CAM_PDN1	CAM_PDN0	CAM_CLK0	DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_SRAM_MODEM_1	DVDD_SRAM_MODEM_1	DVSS	AVSS18_MDPLLGP	AVDD18_MDPLLGP	DVDD_SRAM	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS		SIM2_SCLK	SIM1_SRST	SIM1_SIO	DVDD28_SIM2	AB
AC	CAM_RST0	CAM_RST1		URXD0	CAM_CLK1	DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_SRAM_MODEM	DVSS	DVSS	DVSS	DVDD_SRAM_MODEM_1	DVDD_SRAM_MODEM_1	DVSS	TP_PLLGP	TN_PLLGP	DVDD_SRAM	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	SIM1_SCLK			DVDD_DVFS	AC
AD	EINT4	EINT5	EINT6	UTXD0	EINT2	DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_MODEM	DVDD_MD1	DVSS	DVSS	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP		DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	AD
AE		EINT8			EINT3	DVSS	DVDD_MODEM	DVDD_MODEM	DVSS	DVSS	DVDD_MODEM	DVDD_SRAM_MODEM	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_DVFS	LCM_RST		SDA_APPM	DRVBUS	AE
AF	EINT0	EINT7	KPCOL0	KPCOL1	EINT1	PWM_A	DVDD_MODEM	DVDD_MODEM	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	IDDIG	DSI_TE	DISP_PWM	SCL_APPM		AF
AG	DVDD18_IORB	KPROW0		SPI_MI	SRCLKENAI		DVDD_MODEM	DVDD_MODEM	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	INT_SIM2			SDA3	SCL3	AG
AH		KPROW1	SPI_CLK	SPI_CSB	SPI_MO		DVSS	DVSS	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD	AVSS18_MD			MAIN_X26M_IN						DVSS	DVSS			INT_SIM1	DPI_D1	DPI_D4	DPI_D3	DVDD18_IOLB	AH
AJ	SCL0	SDA0	SCL1	SDA1					PRX_BB1_IP	PRX_BB1_QP							DRX_BB2_QP								BPI_BUS10	BPI_BUS11			DPI_D0		DPI_D5		AJ
AK	PA_VM0	TX_SWAP3		DET_BPI0	MISC_BSI_CK_2	MISC_BSI_CK_3	MISC_BSI_DO_3		PRX_BB1_IN	PRX_BB1_QN	AVSS18_MD	RFIC_ET_P	RFIC_ET_N	AVSS18_MD	DET_BBIP	AVSS18_MD	DRX_BB2_QN	DRX_BB2_IN	DRX_BB2_IP	AVSS18_MD	AVSS18_MD		RFIC0_BSI_D0	RFIC0_BSI_D1	MISC_BSI_CK_0	BPI_BUS9			DPI_D2	DPI_VSYNC	DPI_D6	DPI_D8	AK
AL	PA_VM1	TX_SWAP1	TX_SWAP0	DET_BPI1	MISC_BSI_DO_2	AVSS18_MD	AVSS18_MD	APC1	AVSS18_MD	AVSS18_MD	AVSS18_MD		AVSS18_MD	AVSS18_MD	DET_BBIN	AVSS18_MD	AVSS18_MD		AVSS18_MD	AUXIN2	AUXIN3	AVDD18_MD	RFIC0_BSI_CK		MISC_BSI_DO_0	BPI_BUS8	BPI_BUS6	BPI_ANT0	DPI_CK	DPI_DE	DPI_HSYNC	DPI_D7	AL
AM		TX_SWAP2	BPI_BUS0	BPI_BUS1	BPI_BUS2	AVSS18_MD	DRX_BB1_IP	DRX_BB1_IN		[illegible]	AVSS18_MD	TX_BBQP	TX_BBQN	AVSS18_MD	AVSS18_MD	PRX_BB2_QP	PRX_BB2_QN	AVSS18_MD	AUXIN4	AUXIN0	AUXIN1	AVDD18_AP		RFIC0_BSI_EN	MISC_BSI_CK_1	MISC_BSI_DO_1	BPI_BUS5	BPI_ANT1	BPI_ANT2	DPI_D10	DPI_D11	DVSS	AM
AN	DVSS	DVSS	DVDD18_IOBR		BPI_BUS3	AVDD28_DAC		DRX_BB1_QN	DRX_BB1_QP		TX_BBIP	TX_BBIN		DET_BBQN	DET_BBQP		PRX_BB2_IN	PRX_BB2_IP	AVSS18_MD		REFN	REFP	DVDD18_IOBL	RFIC0_BSI_D2		BPI_BUS7	BPI_BUS4		BPI_ANT3	DPI_D9		DVSS	AN
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

IC Ballout Diff. Table Between MT6755/6752

MT6755 (13.0x13.4mm)



MT6752 (12.6x12.6mm)



Design Notice: I2C Application (1/2)

Set	Controller	Ref. design	Note
I2C0	AP	CTP LCM gate driver	1. Open drain type
I2C1	AP	MEMS sensors Flashlight driver Front camera w/ AF MHL SW charger VBAT boost	1. Open drain type
I2C2	AP	Rear camera w/ AF	1. Open drain type
I2C3	AP	NFC	1. Open drain type
I2C_APPM	AP	MT6311	Dedicated for MT6311 only; does not support 3rd party's I2C device

- A few cameras may lock I2C bus due to large leakage in power off mode. We suggest you use dedicated I2C bus for those cameras.
- I2C address must be unique for the devices shared with the same I2C bus.
- If the camera supports PIP/VIV feature, and AF driver IC is the same, assign different I2C bus for the sub camera.

Design Notice: I2C Application (2/2)

- MT6755 integrates 5 I2C controllers: I2C0, I2C1, I2C2, I2C3 and I2C_APPM

- I2C0 supports 3 I2C mux interfaces (1 dedicate, 2 mux onto other pins)
- I2C1 supports 3 I2C mux interfaces (1 dedicate, 2 mux onto other pins)
- I2C2 supports 2 I2C mux interfaces (1 dedicate, 1 mux onto other pins)
- I2C3 supports only one I2C interface (1 dedicate, no mux onto other pins)
- I2C_APPM supports only one I2C interface (1 dedicate , no mux onto other pins)

External pull-up resistor requirements:

➢ [Compulsory] Add pull-up resistor for open-drain I2C; 4.7K is recommended.

➢ [Optional] Based on your system design, reserve NC pull-up resistor at other muxed I2C.

<table>
<tr><th>Pin name</th><th>Controller</th><th>Pin num</th><th>IO type</th><th>GPIO aux mode</th></tr>
<tr><td>SDA0</td><td rowspan="6">I2C0</td><td></td><td rowspan="2">Open-Drain</td><td>Aux Func.1 (SDA0)</td></tr>
<tr><td>SCL0</td><td></td><td>Aux Func.1 (SCL0)</td></tr>
<tr><td>EINT6</td><td></td><td rowspan="4">Push-Pull</td><td>Aux Func.5 (SDA0)</td></tr>
<tr><td>EINT7</td><td></td><td>Aux Func.5 (SCL0)</td></tr>
<tr><td>F2W_DATA</td><td></td><td>Aux Func.6 (SDA0)</td></tr>
<tr><td>F2W_CLK</td><td></td><td>Aux Func.6 (SCL0)</td></tr>
<tr><td>SDA1</td><td rowspan="6">I2C1</td><td></td><td rowspan="2">Open-Drain</td><td>Aux Func.1 (SDA1)</td></tr>
<tr><td>SCL1</td><td></td><td>Aux Func.1 (SCL1)</td></tr>
<tr><td>IDDIG</td><td></td><td rowspan="4">Push-Pull</td><td>Aux Func.4 (SDA1)</td></tr>
<tr><td>DRVBUS</td><td></td><td>Aux Func.4 (SCL1)</td></tr>
<tr><td>WB_SDATA</td><td></td><td>Aux Func.6 (SDA1)</td></tr>
<tr><td>WB_SEN</td><td></td><td>Aux Func.6 (SCL1)</td></tr>
<tr><td>SDA2</td><td rowspan="4">I2C2</td><td></td><td rowspan="2">Open-Drain</td><td>Aux Func.1 (SDA2)</td></tr>
<tr><td>SCL2</td><td></td><td>Aux Func.1 (SCL2)</td></tr>
<tr><td>SPI_CSB</td><td></td><td rowspan="2">Push-Pull</td><td>Aux Func.5 (SDA2)</td></tr>
<tr><td>SPI_CLK</td><td></td><td>Aux Func.5 (SCL2)</td></tr>
<tr><td>SDA3</td><td rowspan="2">I2C3</td><td></td><td rowspan="2">Open-Drain</td><td>Aux Func.1 (SDA3)</td></tr>
<tr><td>SCL3</td><td></td><td>Aux Func.1 (SCL3)</td></tr>
<tr><td>SDA_APPM</td><td rowspan="2">I2C_APPM</td><td></td><td rowspan="2">Push-Pull</td><td>Aux Func.1 (SDA_APPM)</td></tr>
<tr><td>SCL_APPM</td><td></td><td>Aux Func.1 (SCL_APPM)</td></tr>
</table>

Design Notice: MSDC Application

Set	Function	Power domain	Note
MSDC0	eMMC	DVDD18_MSDC0	1. Dedicated pin for eMMC 2. Independent power domain
MSDC1	T-card	DVDD28_MSDC1	1. Dedicated pin for T-card 2. Independent power domain
MSDC2	MT6630	DVDD18_IORT2	1. PinMux with MT6625L digital pin 2. MT6625L/MT6630 3. 1.8V IO for SDIO3.0

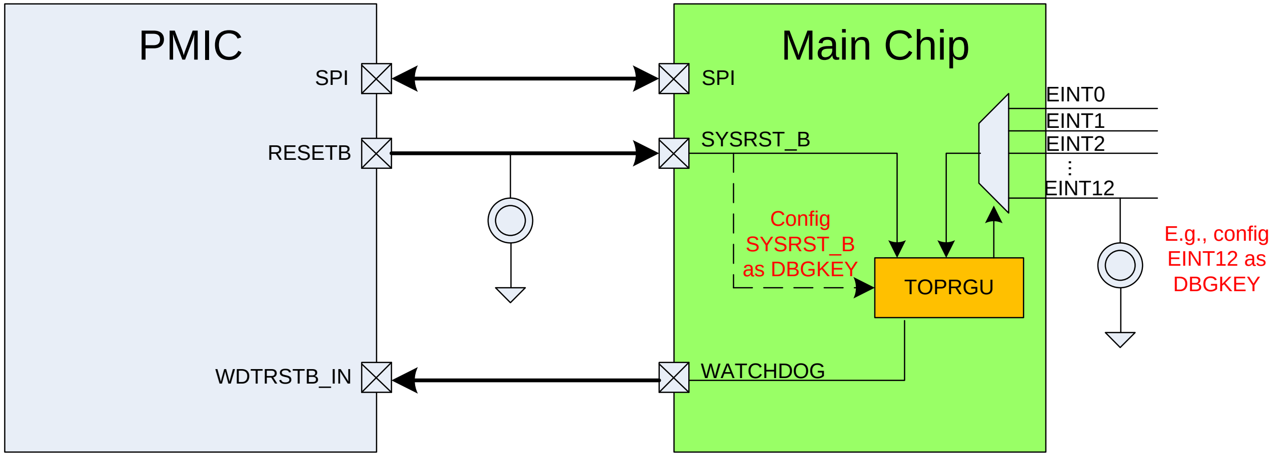
	MT6755	MT6735	MT6752	Common	Unit
VEMC	2.9	3.0	3.0	3.3	V
VIO18	1.8	1.84	1.8	1.8	V
VMCH	3.0	3.0	3.0	3.3	V
VMC (SD3.0)	1.8	1.84	1.8	1.8	V
VMC (SD2.0)	3.0	3.0	3.0	3.3	V

Design Notice: RAMDUMP - External Key Support (1/2)

- Keyword
  - TOPRGU: Top Reset Generation Unit
- Description
  - The original RAMRUMP is triggered only after system hang and reboot through TOPRGU.
  - This new feature supports RAMRUMP triggered by external key (IO).
  - External ramdump debug key feature must use as a test point or reset button, not a real user key; otherwise it will have mis-trigger problem.

Design Notice: RAMDUMP - External Key Support (2/2)

- [Solution A: Recommended] Use one of existing EINT[0:12] pins as debug key
  - The function is default **DISABLED** and can be **reset by TOPRGU.**
  - Input polarity is active **LOW.**
  - EINT DBGKEY has debounce logic.
  - EINT source selection is controlled by TOPRGU.
- [Solution B] Reuse SYSRST_B as debug key (IO)
  - SYSRSTB DBGKEY enable is a **non-reset register.**
  - The function is default **DISABLED.**



GPIO Application Notice

Design Notice: GPIO Selection (1/8)

- Be careful of GPIO with 2.8V power domain for 28nm.
- MT6755 GPIO
  - Supports 190 GPIOs belonging to 11 power domains
  - Power domains of GPIO:
    - DVDD18_IOLT (1.8V)
    - DVDD18_IOLB (1.8V)
    - DVDD18_IOBL (1.8V)
    - DVDD18_IOBR (1.8V)
    - DVDD18_IORB (1.8V)
    - DVDD18_IORT1 (1.8V)
    - DVDD18_IORT2 (1.8V)
    - DVDD18_MSDC0 (1.8V)
    - DVDD28_MSDC1 (1.8V/2.9V)
    - DVDD28_SIM1/DVDD28_SIM2 (1.8V/3.0V)

Design Notice: GPIO Selection (2/8)

- **Pull-up/Pull-down selection**
  - Choose GPIO with suitable PU/PD after reset state for application
    - Example: For "enable pin of audio amplifier", choose GPIO with **PD** after reset state.
    - Example: For "enable pin of external LDO", choose GPIO with **PD** after reset state.

- **Power domain of IO supply selection**
  - Choose GPIO with suitable power domain of IO supply for application.

- **Choose suitable GPIO for peripheral IC**
  - Choose GPIOs with matched direction, pull-up/pull-down, data output, GPIO mode after reset state for peripheral IC application.
  - Select N.C. on Def. Mode for UNUSED PIN, otherwise you may encounter unexpected issue due to wrong setting.

Design Notice: GPIO Selection (3/8)

- **Notice on DCT_Tool usage**

After enabling "InPull En", change the PU/PD value by changing "InPull SelHigh".
(Only valid when GPIO is in input mode)

"InPull En" can enable/disable PU/PD; then GPIO will be the default PU/PD value after reset state.
(Only valid when GPIO is in input mode)

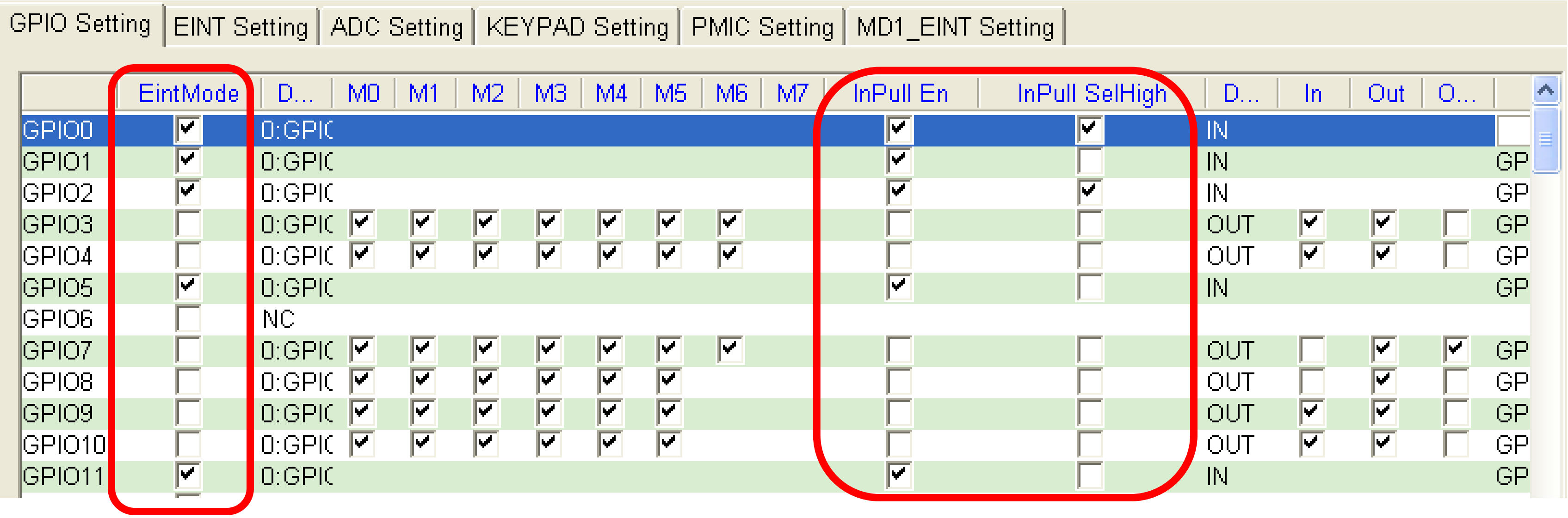
"OutHigh" can change the default output level.
(Only valid when GPIO is in output mode)

GPIO Setting | I2C Setting | CLOCK BUFFER Setting | EINT Setting | ADC Setting | KEYPAD Setting | PMIC Setting | TDSEL/RDSEL | MD1_EINT Setting

	EintMode	Def.Mode	M0	M1	M2	M3	M4	M5	M6	Suspend_State	InPull En	InPull SelHigh	Def.Dir	In	Out	OutHigh
GPIO3	☑	0:GPIO3									☑	☐	IN			
GPIO4	☑	0:GPIO4									☑	☐	IN			
GPIO5	☑	0:GPIO5									☑	☐	IN			
GPIO6	☑	0:GPIO6									☑	☐	IN			
GPIO7	☑	0:GPIO7									☑	☐	IN			
GPIO8	☑	0:GPIO8									☑	☑	IN			
GPIO9	☑	0:GPIO9									☑	☑	IN			
GPIO10	☐	0:GPIO10	☑		☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO11	☐	0:GPIO11	☑		☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO12	☑	0:GPIO12								INPUT_PD	☑	☐	IN			
GPIO13	☐	0:GPIO13	☑		☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO14	☐	0:GPIO14	☑		☑	☐	☐	☐	☐	INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO15	☐	0:GPIO15	☑		☑	☐	☐	☐	☐	INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO16		1:IDDIG	☐	☑	☐	☐	☐				☑	☑				☐
GPIO17		1:SIM1_SCLK	☑	☑	☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO18		1:SIM1_SRST	☑	☑	☑					INPUT_PD	☐	☐	OUT	☑	☑	☐

Design Notice: GPIO Selection (4/8)

- **MT6755 have no dedicated EINT MUX mode.**
  - **GPIO[0:138] can be configured as "External interrupt mode".**
  - **Click EintMode in DCT tool for external interrupt application.**
  - **After EintMode is selected, this pin will be limited for interrupt usage.**
  - **You can set up pull-up or pull-down in "InPullEn" & "InPull SelHigh".**



Design Notice: GPIO Selection (5/8)

- High voltage IO design guide
  - MT6755 (28nm) process IO can sustain 1.8 for general applications.
    - Maximum IO voltage is 1.98V.
  - For application requiring IO voltage over 1.98 volt, 1V8/2V8 IO design is required.
    - Be careful of the schematic design for different applications.
    - DCT tool should be configured properly based on the schematic design.

Improper design or setting will degrade IO reliability.

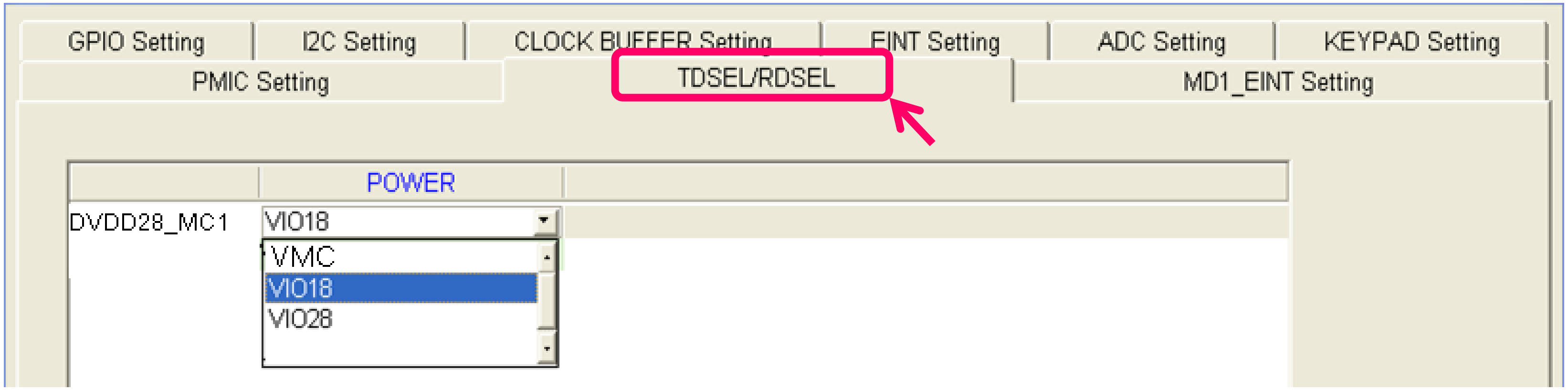
Design Notice: GPIO Selection (6/8)

- High voltage IO overview

No.	Power domain	PMIC suggested IO power connection	Application	Application description
1	**DVDD28_MSDC1**	VMC (MT6351)	1st T-card, embedded SD	Digital 2.9V power input for MSDC1 (1st T-card, embedded SD)
		VIO18 (MT6351)	GPIO_1V8	1V8 GPIO
		VIO28 (MT6351)	GPIO_2V8	2V8 GPIO
2	**AVDD33_USB_P1**	MT6351's VUSB33 (3.3V)	USB	USB 1.1 or USB P1 N.C.
		MT6351's VSIM1 (1.8V/3.0V)	Smart card	IC-USB with device on SIM1
		MT6351's VSIM2 (1.8V/3.0V)	Smart card	IC-USB with device on SIM2

Design Notice: GPIO Selection (7/8)

- **High voltage IO DCT configuration**
  - **Defined in DCT tool TDSEL/RDSEL Setting page**
    - “**DVDD28_MSDC1**” is applied to define the voltage level of MSDC1_CMD/CLK/DAT[0:3]. For T-card/embedded SD application, select VMC.



Design Notice: GPIO Selection (8/8)

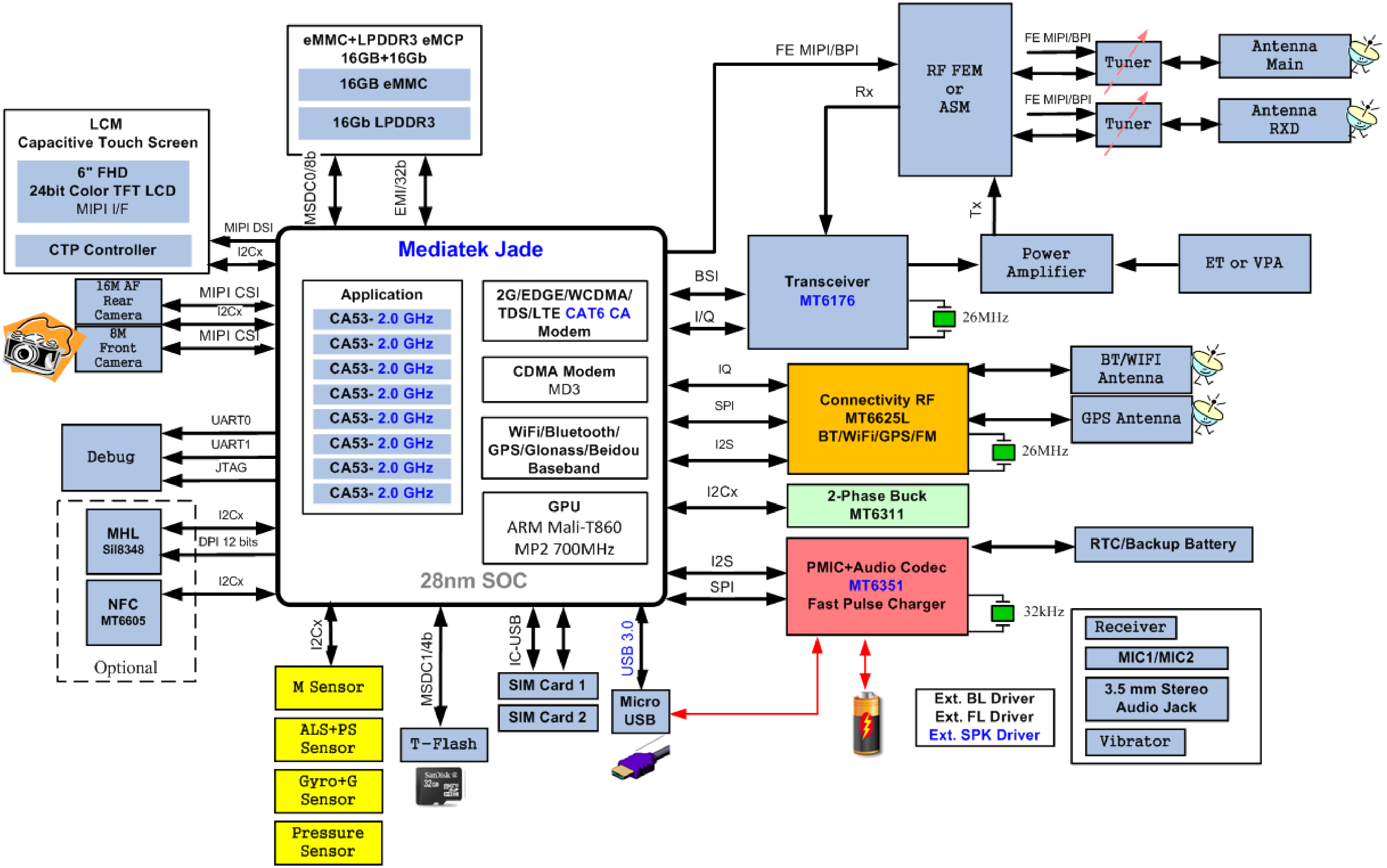
- MT6755 supports x139 EINTs
  - **GPIO[0:138]** can be configured as “External interrupt mode”.
- Only EINT[0:15] supports HW de-bounce.

EINT Ports	De-bounce	De-bounce time
EINT [0:15]	HW based	0.125/0.25/0.5/1/16/32/64/128/256/512 ms
EINT [16:138]	SW based	1/16/32/64/128/256/512 ms

- Please refer to MT6755_GPIO_Formal_Application_Spec.

SCH Design Notice

MT6755 System Block

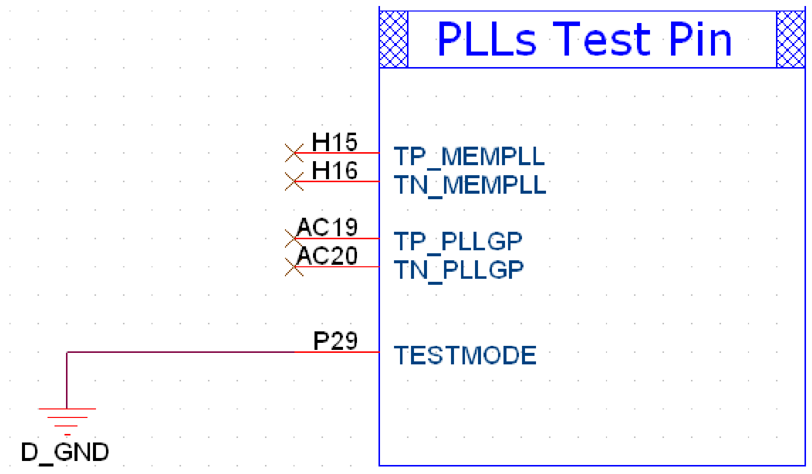


Schematic Notice: Mode Selection

- **Test mode selection**

Chip #	Pin name	Pin out	Normal mode	TEST mode
MT6755	TESTMODE	P29	GND	VIO18 (1.8V)

- For normal usage, configure the pins above to "normal mode".
- TESTMODE is only for debugging. Follow the configuration above.



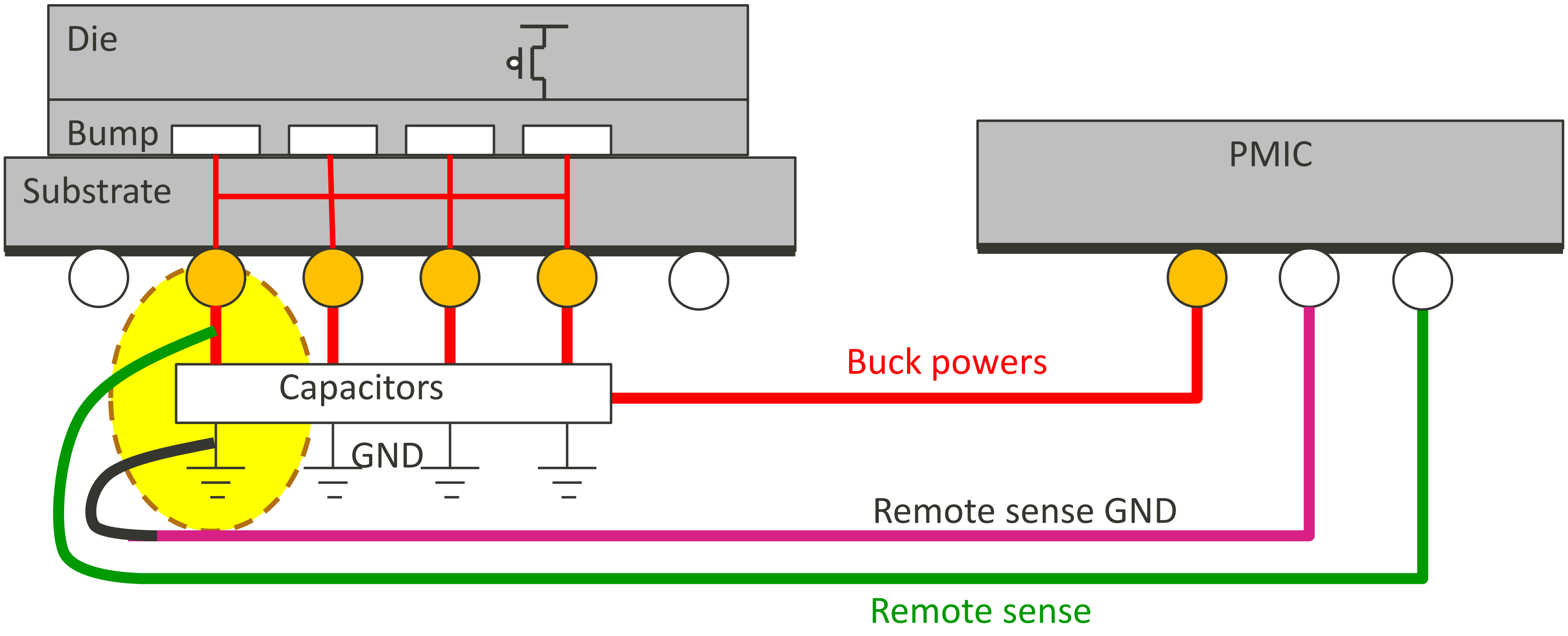
Schematic Notice: Core Powers (1/3)

- There are eight core power rails which should follow MMD or pass PDN simulation, including VPROC, VCORE, VGPU, VMD1, VMODEM, VM, VSRAM and VSRAM_MODEM.
- VPROC, VCORE, VGPU, VMD1, VMODEM, VM, VSRAM and VSRAM_MODEM are powered by dedicated bulk and LDO power source from PMIC (MT6311 & MT6351) respectively.

MT6735 core powers	PMIC power source	Buck/LDO	Min. voltage	Max. voltage
VPROC (DVDD_DVFS)	MT6311's VSW1/2	2-phase Buck	0.6	1.4
VCORE (DVDD_TOP)	MT6351's VCORE	Buck	0.7	1.31
VGPU (DVDD_MFG)	MT6351's VGPU	Buck	0.7	1.31
VMD1 (DVDD_MD1)	MT6351's VMD1	Buck	0.6	1.2
VMODEM (DVDD_MODEM)	MT6351's VMODEM	Buck	0.6	1.2
VM (DDRV & DDRV_CLK)	MT6351's VDRAM	LDO	0.9	1.21
VSRAM (DVDD_SRAM)	MT6351's VSRAM_PROC	LDO	0.6	1.2
VSRAM_MODEM (DVDD_SRAM_MODEM & DVDD_SRAM_MODEM_1)	MT6351's VSRAM_MD	Buck	0.6	1.2

Schematic Notice: Core Powers (2/3)

- Remote sense design of buck powers (1/2)
  - The remote sense connection of buck powers should be close to MT6755's specific power ball (defined on the next page).



Schematic Notice: Core Powers (3/3)

Remote sense design of buck powers (2/2)

- Differential pair of VPROC remote sense should be close to MT6755's DVDD_DVFS ball.
- Differential pair of VCORE remote sense should be close to MT6755's DVDD_TOP ball.
- Differential pair of VGPU remote sense should be close to MT6755's DVDD_MFG ball.
- Differential pair of VMD1 remote sense should be close to MT6755's DVDD_MD1 ball.
- Differential pair of VMODEM remote sense should be close to MT6755's DVDD_MODEM ball.
- Differential pair of VSRAM_MODEM remote sense should be close to MT6755's DVDD_SRAM_MODEM ball.

MT6755 core powers	PMIC power source	PMIC power remote sense pin	MT6755 power ball sensed
VPROC (DVDD_DVFS)	MT6311's VSW1/2	VFBP (E2)/VFBN (D2)	DVDD_DVFS
VCORE (DVDD_TOP)	MT6351's VCORE	VCORE_FB (E4)/ GND_VCORE_FB (E5)	DVDD_TOP
VGPU (DVDD_MFG)	MT6351's VGPU	VGPU_FB (E14)/ GND_VGPU_FB (D14)	DVDD_MFG
VMD1 (DVDD_MD1)	MT6351's VMD1	VMD1_FB (E3)/ GND_VMD1_FB (D3)	DVDD_MD1
VMODEM (DVDD_MODEM)	MT6351's VMODEM	VMODEM_FB (C1)/ GND_VMODEM_FB (B1)	DVDD_MODEM
VSRAM_MODEM (DVDD_SRAM_MODEM & DVDD_SRAM_MODEM_1)	MT6351's VSRAM_MD	VSRAM_MD_FB (D2)/ GND_VSRAM_MD_FB (D1)	DVDD_SRAM_MODEM

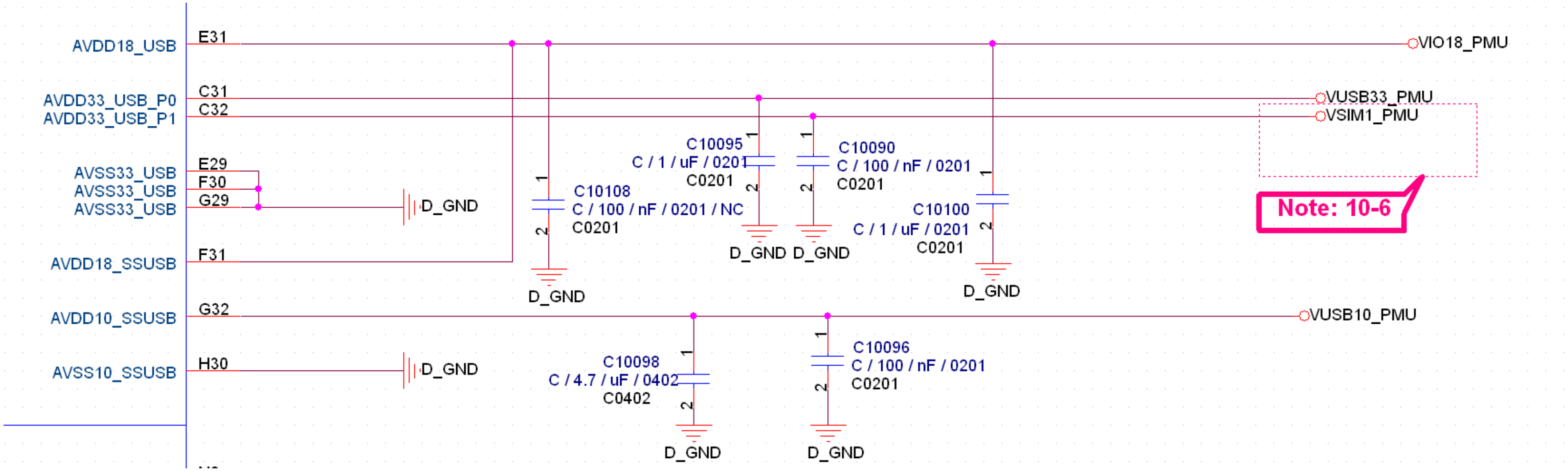
Schematic Notice: Analog Power (1/2)

Power	Powered by	De-coupling + power cap.	Function
AVDD18_MD	VIO18	1uF	Analog power input 1.8V for BBTX, BBRX
AVDD18_AP			Analog power input 1.8V for AUXADC, TSENSE
AVDD28_DAC	**VTCXO28**	0.1uF	Analog power input 2.8V for APC
AVDD18_DDR	VIO18	0.1uF	Analog power input 1.8V for PLL
AVDD18_MDPLLGP	VIO18	1uF	Analog power input 1.8V for PLL
AVDD18_MIPITX	VIO18	1uF	Analog power for MIPI DSI 4 Lane
AVDD18_MIPIRX0	VIO18	1uF	Analog power for MIPI CSI0 4 Lane
AVDD18_MIPIRX1			Analog power for MIPI CSI1 4 Lane
AVDD18_USB	VIO18	1uF	Analog power 1.8V for USB P0/P1/USB HS
AVDD18_SSUSB			Analog power 1.8V for USB 3.0
AVDD33_USB_P0	VUSB33	1uF	Analog power 3.3V for USB/USB FS
AVDD33_USB_P1	**VSIM1 (IC-USB)**	0.1uF	Analog power 3.3V for USB/USB FS/IC-USB
	VUSB33	0.1uF	Analog power 3.3V for USB P1 N.C.
AVDD10_SSUSB	VUSB10	4.7uF + 0.1uF	Analog power 1.0V for USB 3.0
AVDD18_WBG	**VCN18**	0.1uF	Analog power 1.8V for WBG (MT6625L)
	VIO18	0.1uF	Digital power 1.8V for CONN_IO (MT6630)

Schematic Notice: Analog Power (2/2)

- AVDD33_USB_P0 supports USB_HS/USB_FS/OTG.
- AVDD33_USB_P1 supports USB_FS/IC-USB.

Power in	Application	Power source
AVDD33_USB_P0	USB_HS/USB_FS/OTG	MT6351's VUSB33 (3.3V)
AVDD33_USB_P1	USB_FS	MT6351's VUSB33 (3.3V)
	IC-USB with device on SIM1	MT6351's VSIM1 (1.8V/3.0V)
	IC-USB with device on SIM2	MT6351's VSIM2 (1.8V/3.0V)



Schematic Notice: General Power

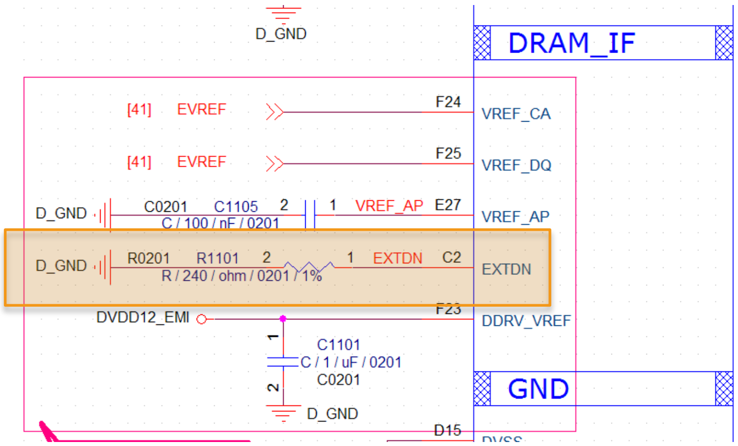
- High speed IO bypass cap. should be of high priority (close to BB).
  - High speed IO bypass cap. should be put close to MT6755.

Power domain	Power by	IO characteristic	Bypass cap.	Function
DVDD18_IOLT DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2	VIO18 (MT6351)	Low speed	0.1 uF*7	Digital 1.8V power input for IO
DVDD18_MSDC0	VIO18 (MT6351)	**High speed**	0.1 uF	Digital 1.8V power input for MSDC0
DVDD28_MSDC1	VMC (MT6351)	**High speed**	1uF	Digital 1.8V/2.9V power input for MSDC1
DVDD18_MC1	VIO18 (MT6351)	Low speed	0.1 uF	Digital 1.8V power input for 3.3V IO
DVDD28_SIM1	VSIM1 (MT6351)	Low speed	0.1 uF	Digital 1.8V/3.0V power input for SIM1
DVDD28_SIM2	VSIM2 (MT6351)	Low speed	0.1 uF	Digital 1.8V/3.0V power input for SIM2
DVDD18_SIM	VIO18 (MT6351)	Low speed	x	Digital 1.8V power input for 3.3V IO

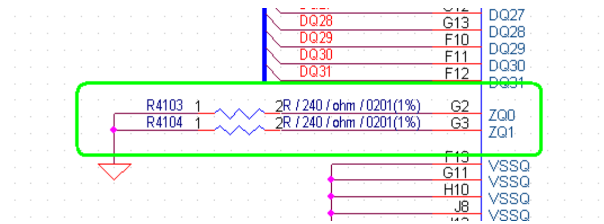
Schematic Notice: DRAM Application (1/3)

Driving strength calibration resistor

MT6755



DRAM

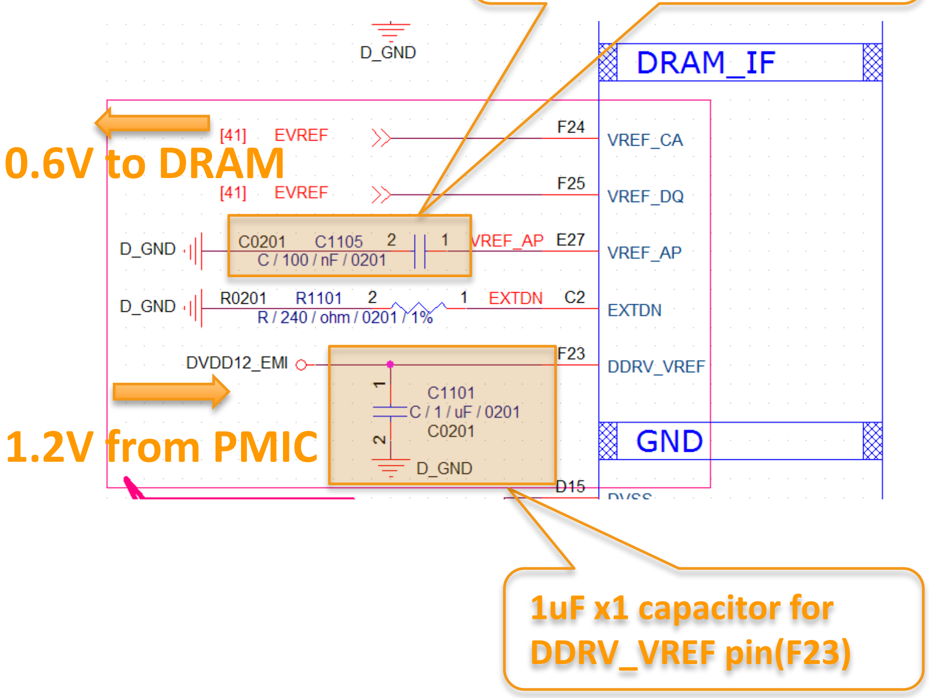


MT6755 EXTDN & DRAM ZQx resistor = 240ohm (1%)

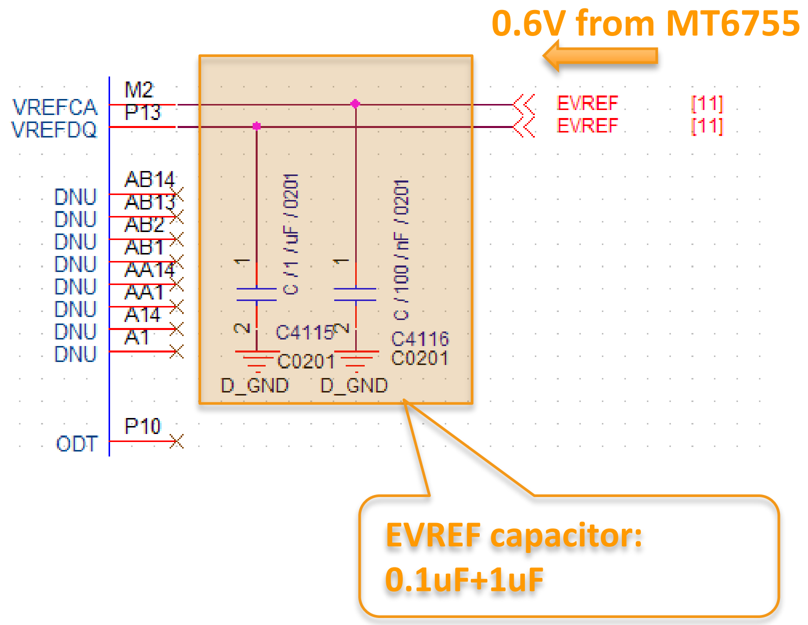
Schematic Notice: DRAM Application (2/3)

VREF (reference voltage)

MT6755



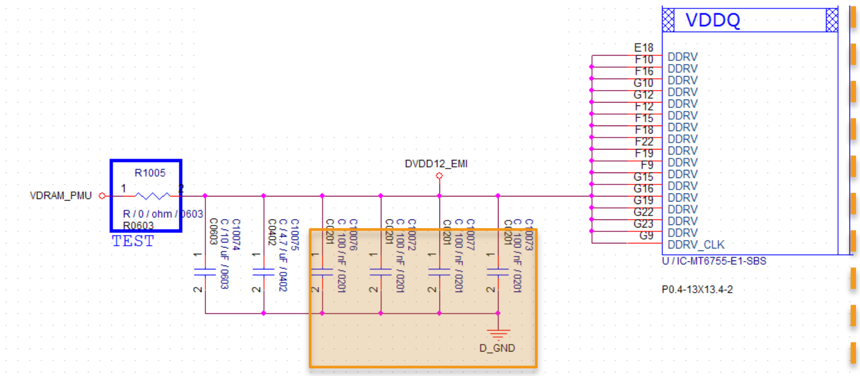
DRAM



Schematic Notice: DRAM Application (3/3)

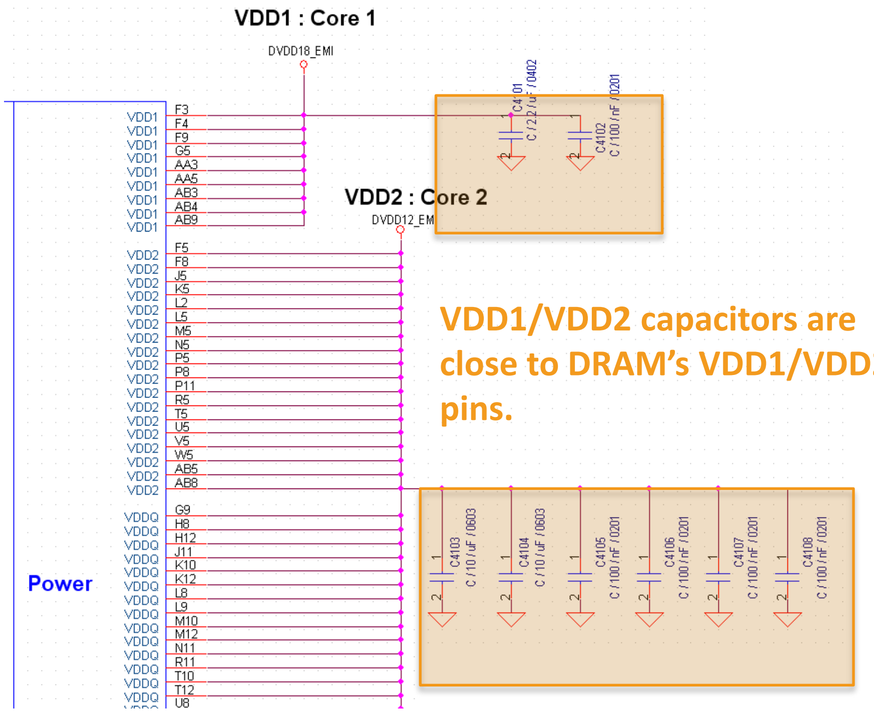
IO Power

MT6755



0.1uF x4 are close to MT6755's DDRV pins.

DRAM



VDD1/VDD2 capacitors are close to DRAM's VDD1/VDD2 pins.

Schematic Notice: eFUSE (1/2)

- **eFUSE programming**

Chip #	Pin name	Pin out	Normal mode	Program mode
MT6755	DVDD_VQPS	B30	GND	VEFUSE (Max 1.98V)

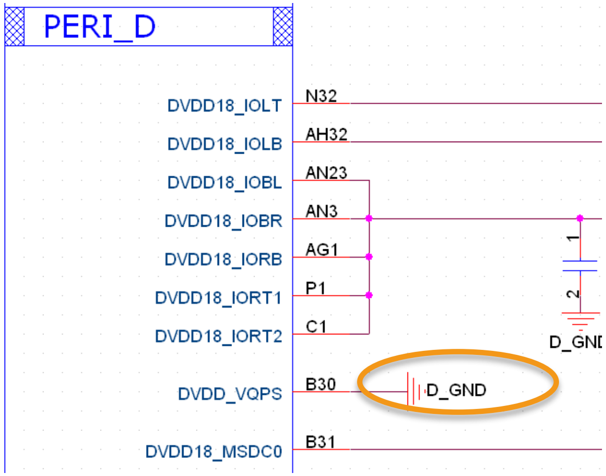
- For normal usage, configure the pin above to “normal mode”.
- MT6755 eFuse programming has high-voltage stress time constraint; the maximum accumulative time of eFUSE programming when “DVDD_VQPS” =1.8V~1.98V should be shorter than 0.2 sec. (PMIC general LDO VEFUSE)

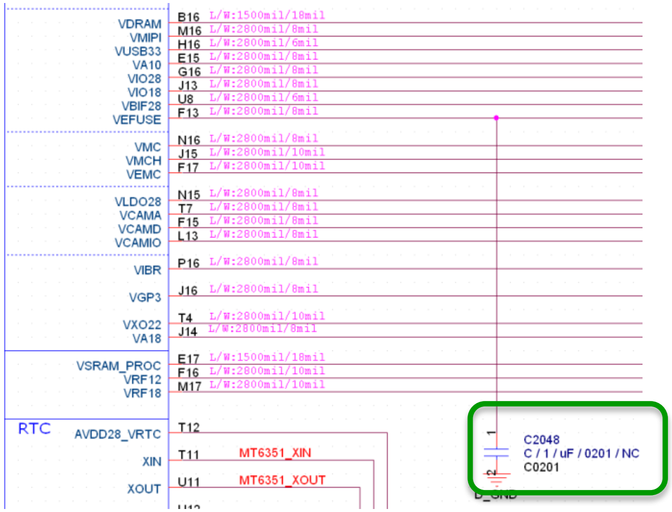
- **eFUSE programming specification**
  - **Voltage: Typical 1.8V (1.8V ~ 1.98V)**
  - **Programming time: ~12us**
  - **Current consumption: ~100mA**

Note: VEFUSE power (from PMIC) must be added with 1uF bypass cap.
*In no burning eFUSE case, tie pin DVDD_VQPS to GND -> Bypass CAP can be NC or removed.
*If burning eFUSE case is required, pin DVDD_VQPS should be connected to VEFUSE -> Bypass CAP should be 1uF.

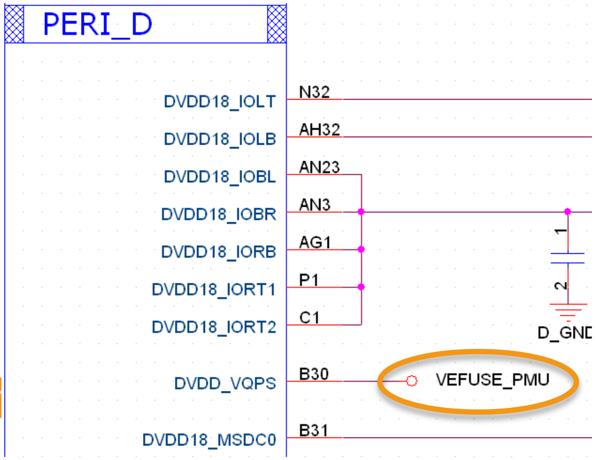
Schematic Notice: eFUSE (2/2)

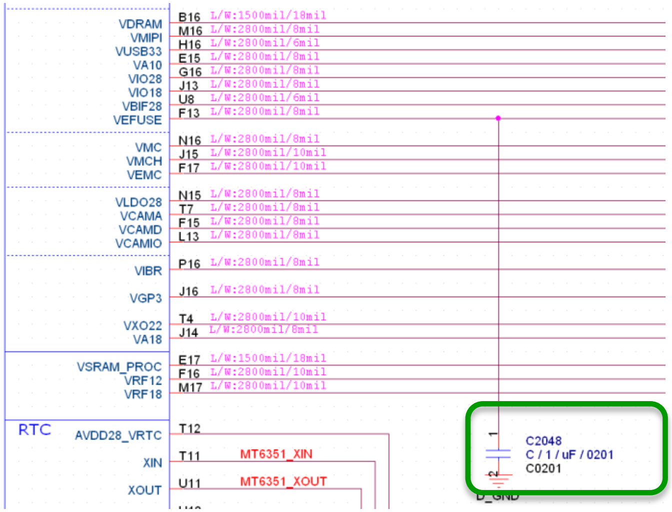
- VEFUSE power (from PMIC) must be added with 1uF bypass cap
  - In no burning eFUSE case, tie pin DVDD_VQPS to GND.
    → Bypass cap can be NC or removed.



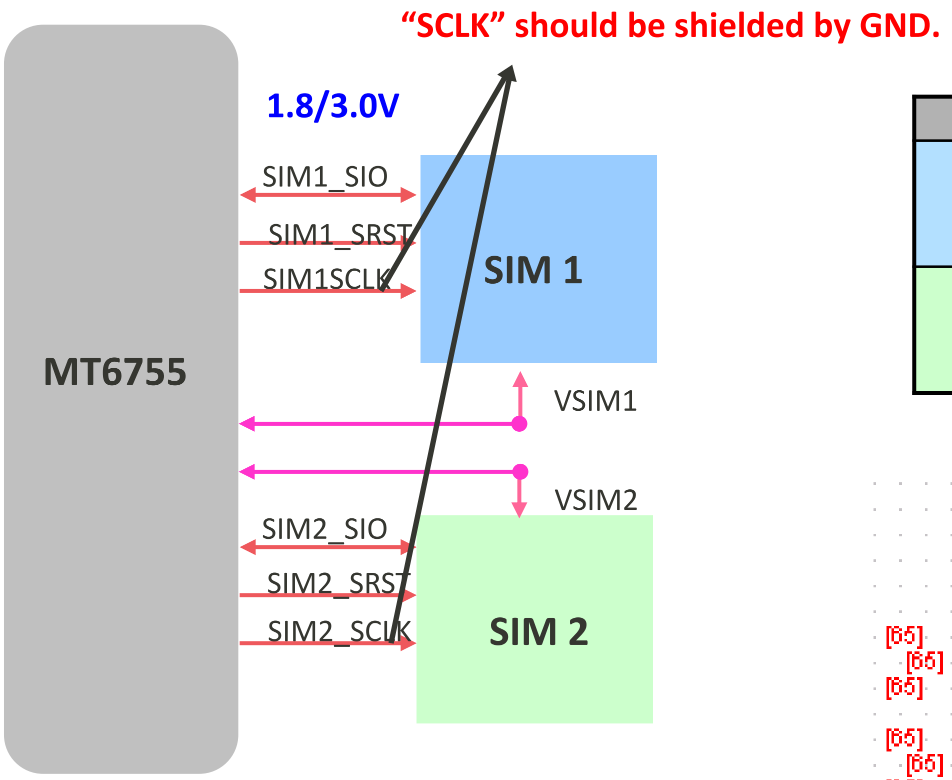


  - If burning eFUSE case is needed, pin DVDD_VQPS should be connected to VEFUSE
    →Bypass cap should be 1uF.

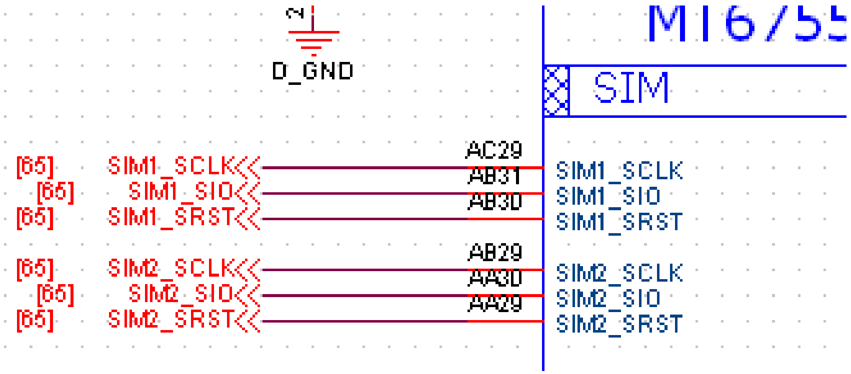




Schematic Notice: Dual SIM Application



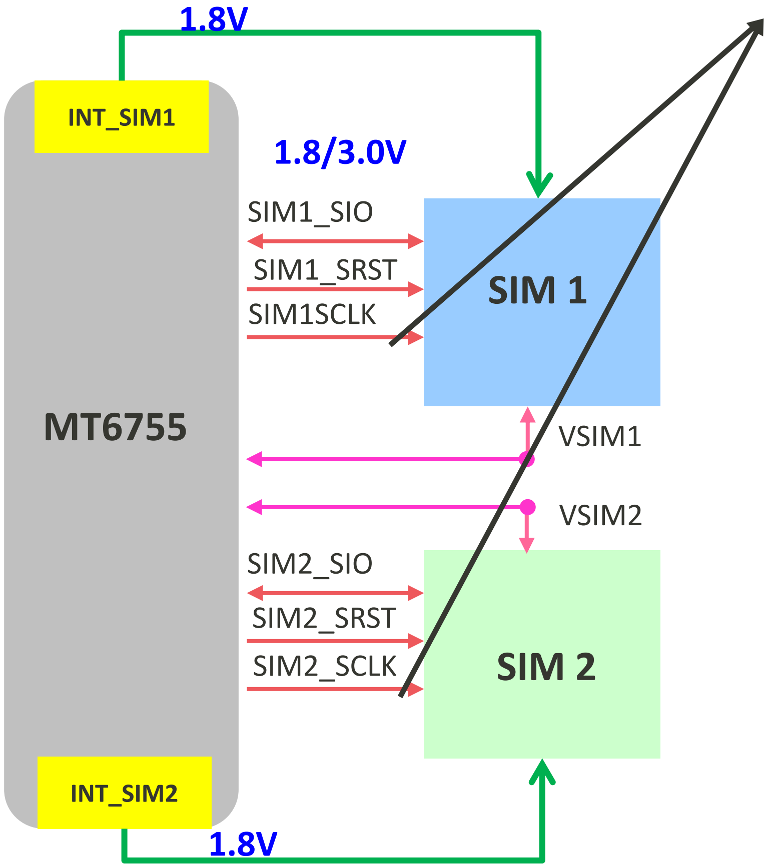
	MT6755pin	Name
SIM1	AC29	SIM1_SCLK
	AB30	SIM1_SRST
	AB31	SIM1_SIO
SIM2	AB29	SIM2_SCLK
	AA29	SIM2_SRST
	AA30	SIM2_SIO



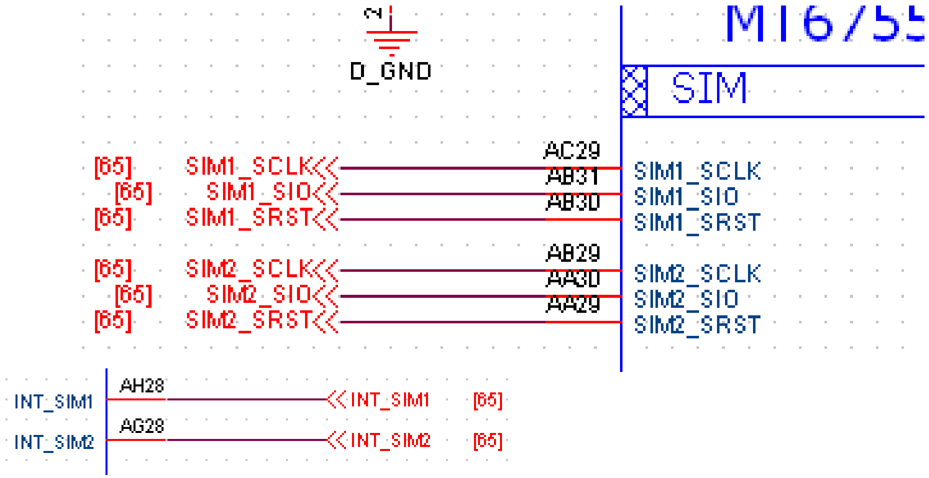
Schematic Notice: SIM Hot Plug (1/2)

- MT6755 supports dual SIM hot plug.

"SCLK" should be shielded by GND.



	MT6755Pin	Name
SIM1	AC29	SIM1_SCLK
	AB30	SIM1_SRST
	AB31	SIM1_SIO
	AH28	INT_SIM1
SIM2	AB29	SIM2_SCLK
	AA29	SIM2_SRST
	AA30	SIM2_SIO
	AG28	INT_SIM2



Schematic Notice: SIM Hot Plug (2/2)

- MT6755 INT selection for SIM hot plug:

  - For SIM1 hot plug, select ball with pin mux.

  I0:MD_INT1_C2K_UIM0_HOT_PLUG, e.g. INT_SIM1, DPI_D7, CAM_CLK1

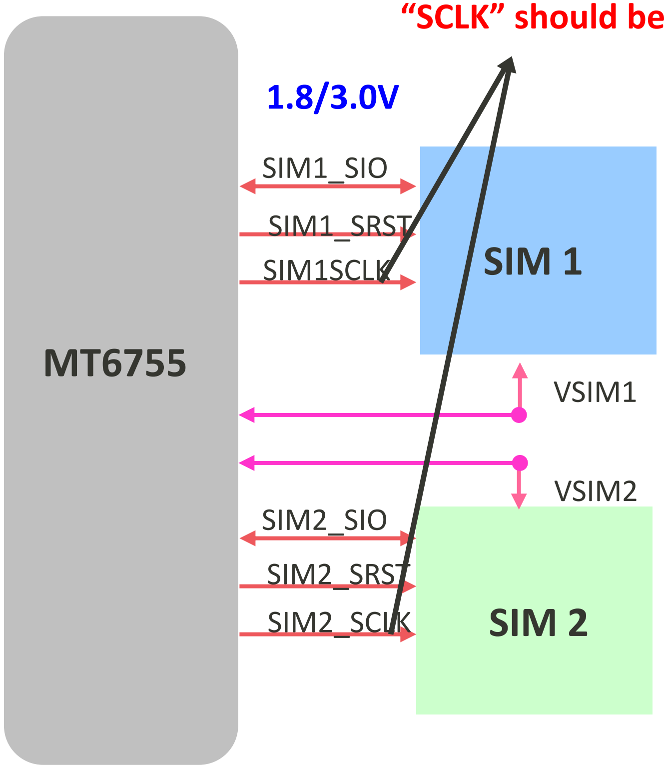
  - For SIM2 hot plug, select ball with pin mux.

  I0:MD_INT2_C2K_UIM1_HOT_PLUG, e.g. INT_SIM2, DPI_D6, PWM_A

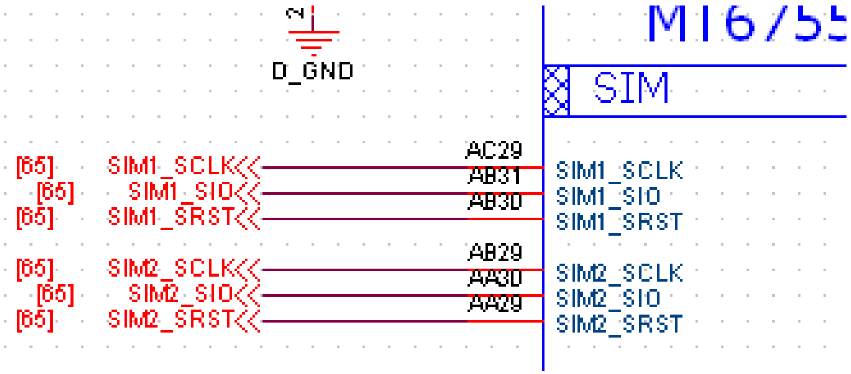
Pin Name	GPIO reset default mode	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7
DPI_D6	0	EINT19	**GPIO19**	O*DPI_D6	I1:URXD1	O:CONN_MCU_TDO	I0:MD_INT2_C2K_UIM1_HOT_PLUG		O:I2S1_LRCK	B0:DBG_MON_A25
DPI_D7	0	EINT20	**GPIO20**	O*DPI_D7	O:UTXD1	O:CONN_MCU_DBGAC	I0:MD_INT1_C2K_UIM0_HOT_PLUG		O:I2S1_DO	B0:DBG_MON_A26
INT_SIM2	0	EINT45	**GPIO45**	I0:MD_INT2_C2K_UIM1	I1:URXD1	I1:UCTS1	O*CLKM0		I1:IDDIG	B0:DBG_MON_A17
INT_SIM1	0	EINT46	**GPIO46**	I0:MD_INT1_C2K_UIM0	O:UTXD1	O:URTS1	O:PWM_B		O:USB_DRVVBUS	B0:DBG_MON_A18
PWM_A	0	EINT100	**GPIO100**	O:PWM_A	I1:URXD1	I0:MD_INT0	O*CLKM3	I0:MD_INT2_C2K_UIM1	O:ANT_SEL4	B0:DBG_MON_A35
CAM_CLK1	0	EINT109	**GPIO109**	O*CMMCLK1	O:PWM_C	I0:MD_INT0	I0:CONN_MCU_AICE_T	I0:MD_INT1_C2K_UIM0	O:CMFLASH	B0:DBG_MON_A9

Schematic Notice: Dual SIM Application

"SCLK" should be shielded by GND.

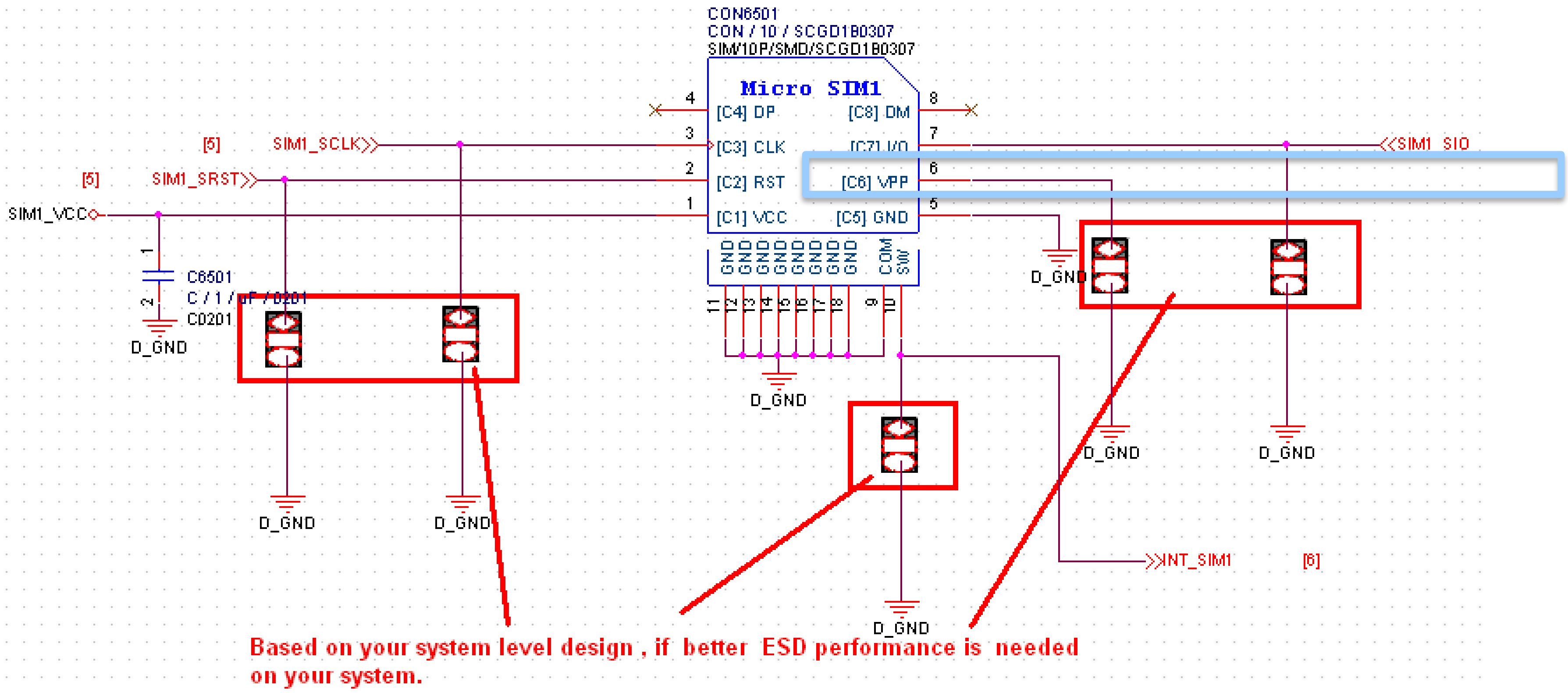


	MT6755pin	Name
SIM1	AC29	SIM1_SCLK
	AB30	SIM1_SRST
	AB31	SIM1_SIO
SIM2	AB29	SIM2_SCLK
	AA29	SIM2_SRST
	AA30	SIM2_SIO



Schematic Notice: Without NFC Application

If your project doesn't have NFC function, VPP[C6] should be NC.(Do NOT connect to VCC[C1])



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For more information on SIM generic design notice, refer to DCC.

(.. > HW > Common Design Notes > SIM)

Schematic Notice: LCM Application (1/8)

- MT6755 features

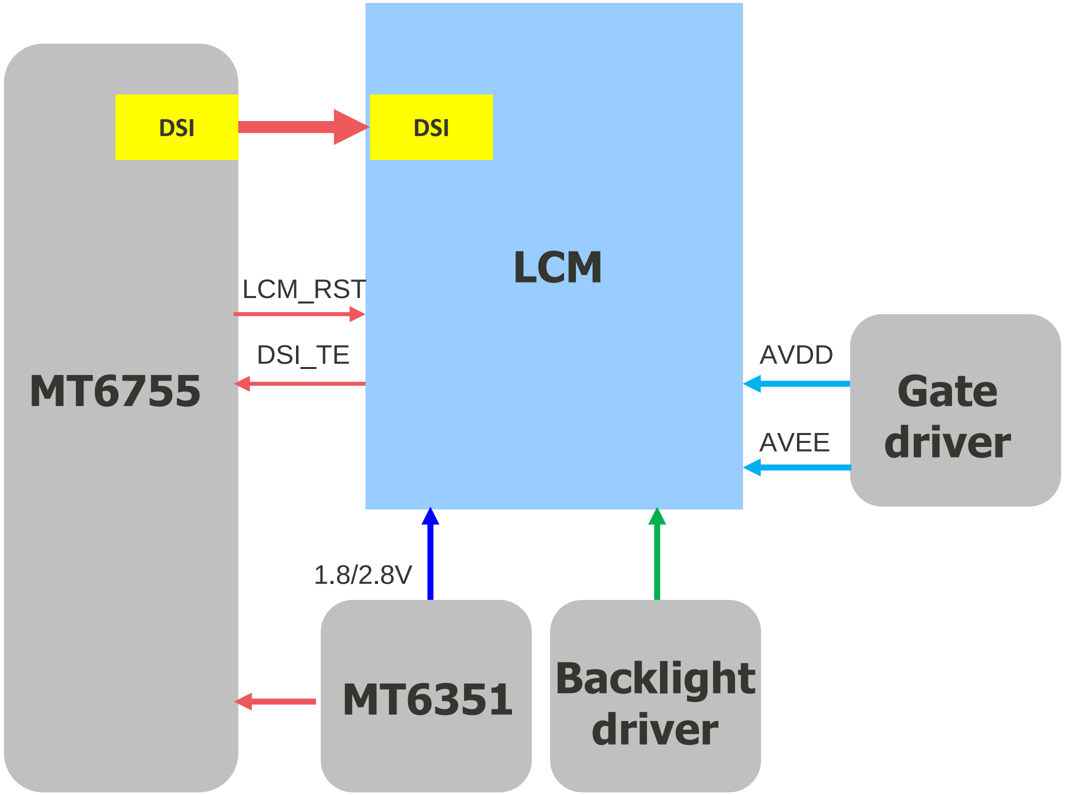
	MT6732	MT6752	MT6753	MT6755
Display	**HD720 1280x720**	**FHD1080 1920x1080**	**FHD1080 1920x1080**	**FHD1080 1920x1080**
Lane #	4, 1.2Gbps/Lane	4, 1.2Gbps/Lane	4, 1Gbps/Lane	4, 1.2Gbps/Lane

- Interface
  - Supports MIPI DSI command/video mode, 4-lane interface
  - Dedicated HW tearing free control pin for MIPI DSI interface

- IO power
  - Supports 1.8V IO level LCM (AVDD18_MIPITX, pin H32)

Schematic Notice: LCM Application (2/8)

- LCM side design notice
  - 4 Lane x1 BB and LCM side
  - 4 Lane LCMx1



Schematic Notice: LCM Application (3/8)

- LCM side design notice
  - Power
    - 2 power mode

      AVDD (VCI): Connect to 2.8V for LCM analog power

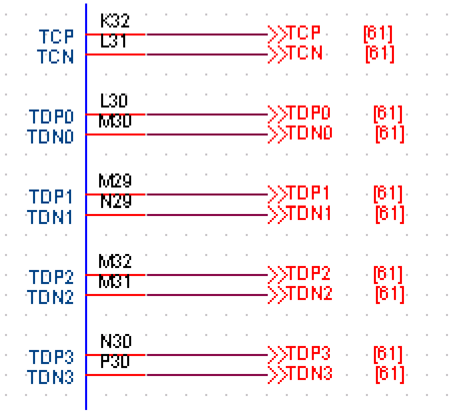
      IOVDD: Connect to 1.8V for LCM I/O power
    - 3 power mode

      IOVDD: Connect to 1.8V for LCM I/O power

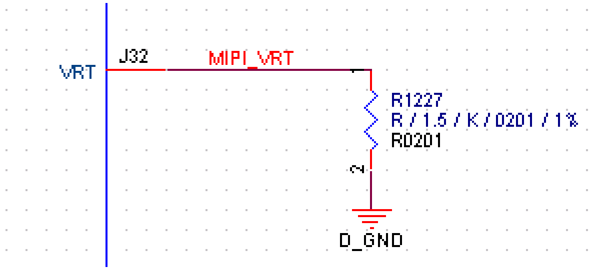
      AVDD/AVEE: Connect to external LCM gate drive
  - LCM data
    - All LCM data pin are reserved at BB side.
  - CABC
    - Connect LCM BLC pin or MT6755 DISP_PWM pin to external backlight driver.
  - System performance
    - EMI filter/common choke over LCM control pin and data bus are optional (trade-off between performance and cost). It can be reserved in the 1st version SMT.

Schematic Notice: LCM Application (4/8)

- MIPI DSI
  - Dedicated MIPI DSI 4-lane interface
  - If MIPI DSI function is used, the unused pins can not be used as GPI



  - MIPI PHY uses ref. current source resistor 1.5K (1%) that should be placed close to MT6755.



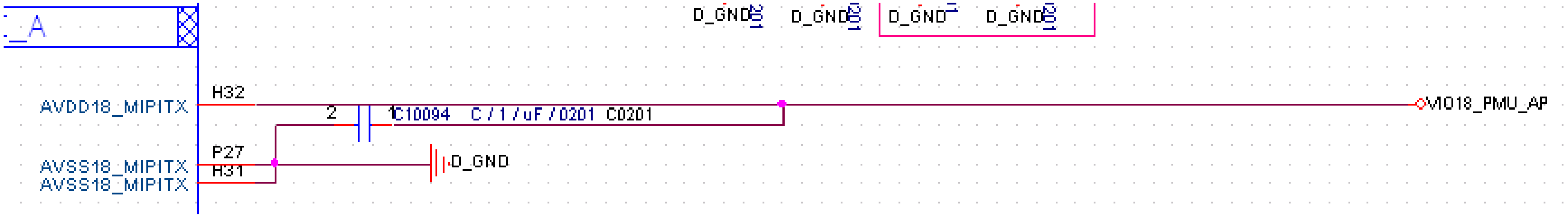
Schematic Notice: LCM Application (5/8)

- BB side design notice
  - MIPI DSI interface contributes to the simplicity of system design.
  - MIPI DSI CLK/DATA are differential pair, and the trace layout should meet 100ohm differential impedance.
    - MIPI_TCP/MIPI_TCN
    - MIPI_TDP0/MIPI_TDN0
    - MIPI_TDP1/MIPI TDN1
    - MIPI_TDP2/MIPI TDN2
    - MIPI_TDP3/MIPI TDN3

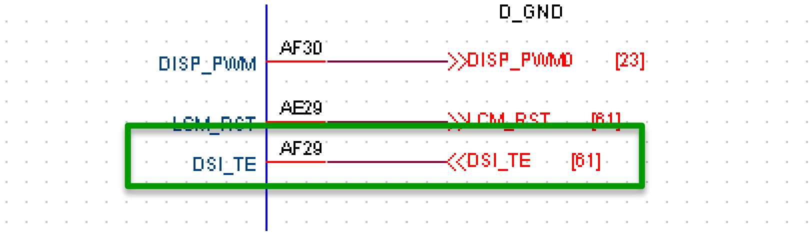
GPIO No.	Name	MT6755 pin
GPIO146	TDN3	P30
GPIO145	TDP3	N30
GPIO144	TDN2	M31
GPIO143	TDP2	M32
GPIO142	TCN	L31
GPIO141	TCP	K32
GPIO140	TDN1	N29
GPIO139	TDP1	M29
GPIO138	TDN0	L30
GPIO137	TDP0	M30

Schematic Notice: LCM Application (6/8)

- Connect all MIPI power domain to 1.8V.
- Bypass cap for MIPI power domain should be close to BB chip.



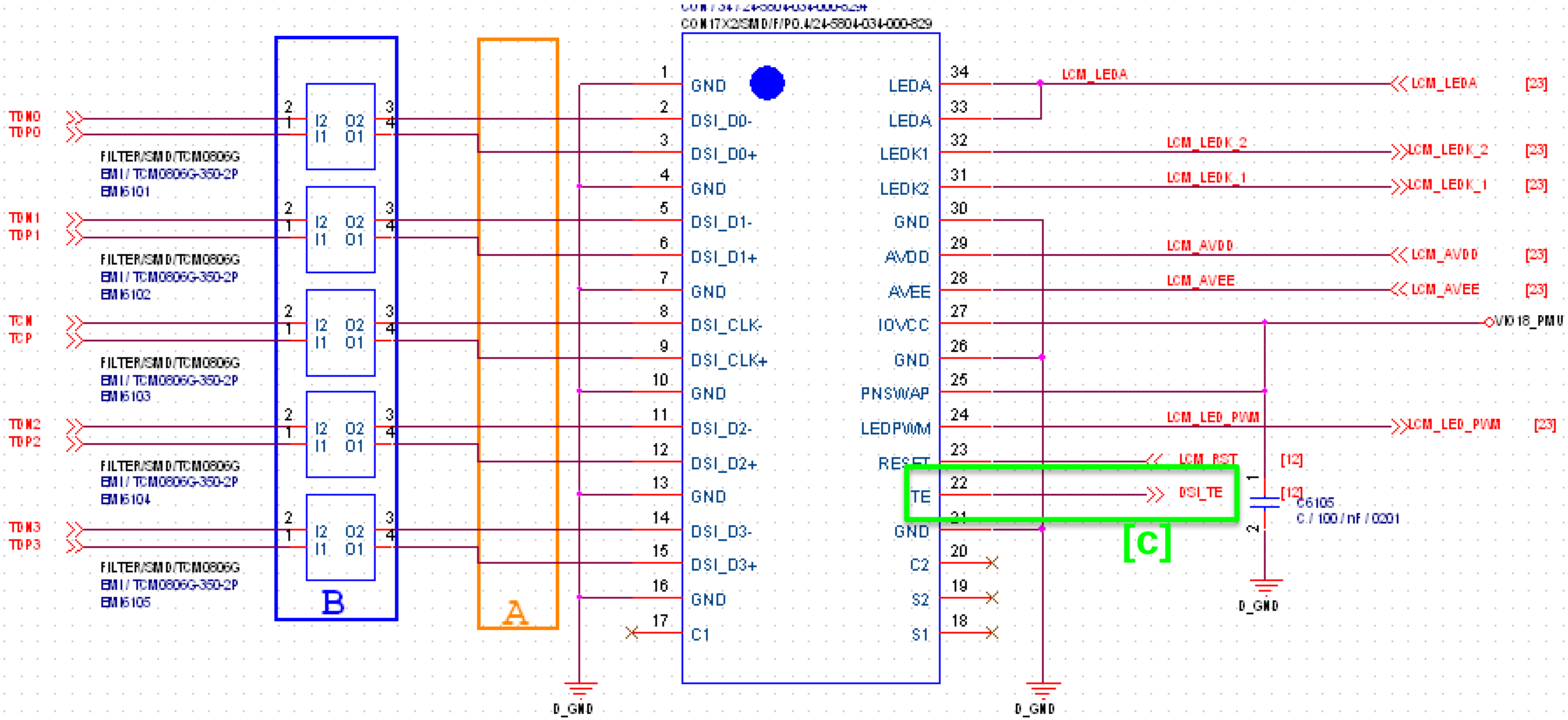
- DSI_TE MUST be connected to LCM TE Pin.



Schematic Notice: LCM Application (7/8)

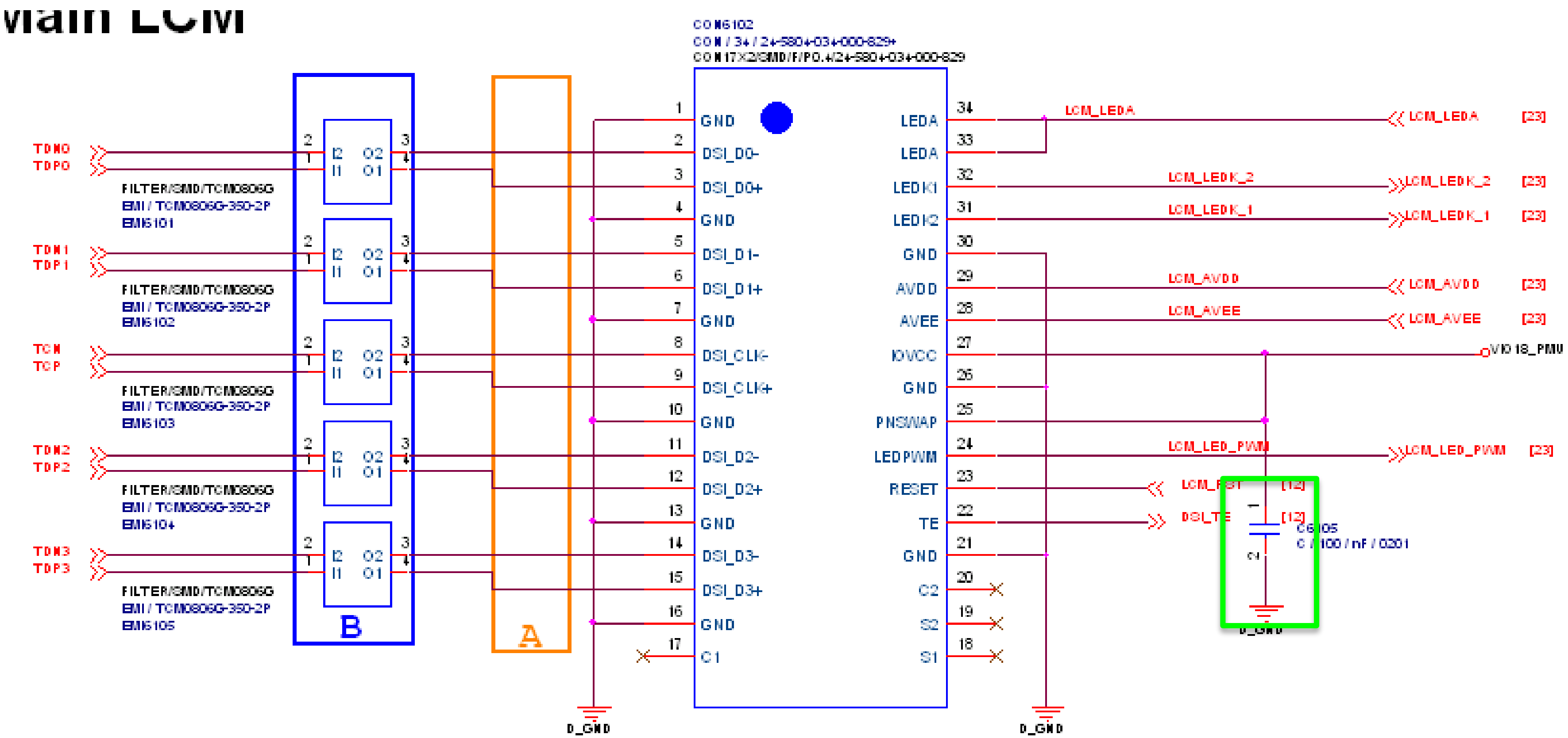
– MIPI DSI interface

- We suggest you insert a ground (G) signal between differential pairs to improve inter-lane cross coupling. [A]
- We suggest you reserve common-mode choke to prevent RF de-sense. The max. cap loading of common-mode choke should be less than 3pF. [B]
- Dedicated HW tearing free control pin for MIPI DSI interface , LCM TE MUST be connected to DSI_TE.[C]



Schematic Notice: LCM Application (8/8)

– Power supply
  - IOVCC of LCM module is powered by PMU’s VIO18_PMU.
  - Reserve 100nF capacitor on the power rails of LCM with shunt connection. This capacitor should be placed close to LCM connector.
  - AVDD/AVEE of LCM module is powered by 3rd party chip (e.g. NT50358/TPS65132).



For more information on LCM generic design notice, refer to DCC.

(.. > HW > Common Design Notes > Display)

Schematic Notice: Camera (1/10)

- MT6755 features:

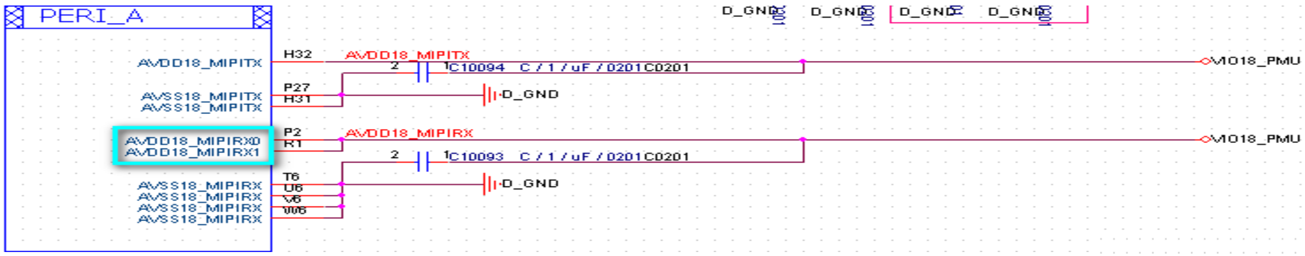
	MT6732	MT6752	MT6755
Rear camera	13M@30fps	16M@30fps	16M@30fps
Lane #	4, 1.5Gbps/Lane	4, 1.5Gbps/Lane	4, 1.5Gbps/Lane
Front camera	13M@30fps	16M@30fps	16M@30fps
Lane #	4, 1.5Gbps/Lane	4, 1.5Gbps/Lane	4, 1.5Gbps/Lane

- Interface
  - Supports MIPI CSI-2, 4-lane interface for rear camera
  - Supports MIPI CSI-2, 4-lane interface for front camera

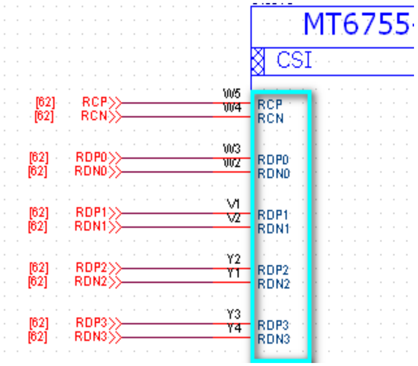
- IO power
  - Supports 1.8V IO level rear camera (AVDD18_MIPIRX0 (N30))
  - Supports 1.8V IO level front camera (AVDD18_MIPIRX1 (W31))

Schematic Notice: Camera (2/10)

- MT6755 image sensor interfaces – MIPI “CSI-2” (1/2)
  - Power
    - **Power name:** AVDD18_MIPIRX & AVDD18_MIPITX.
      - Front-facing (sub-camera) and rear-facing camera (main) camera interfaces are powered by AVDD18_MIPIRX0 and AVDD18_MIPIRX1.



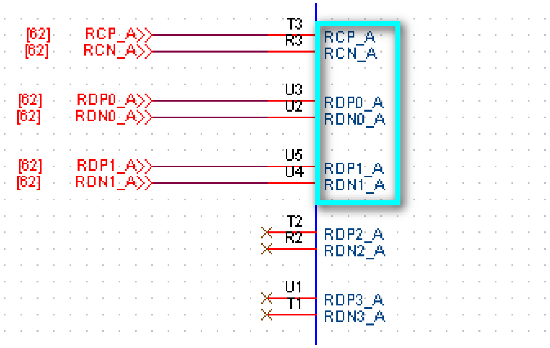
  - MIPI “CSI-2” four-lane interface for rear-facing (main) camera
    - Differential pair of MIPI CSI, 4-lane:
      - RCP/RCN
      - RDP0/RDN0; RDP1/RDN1
      - RDP2/RDN2; RDP3/RDN3



    - The data lane number of MIPI “CSI-2” 4-lane can be configured to support 1, 2 or 4 lanes.
      - Signals to support 1~n data lane, where n= 4:
        { RCP / RCN } ; { RDP0 / RDN0 } to { RDP(n-1) / RDN(n-1) }
    - The data receiving throughput of MIPI “CSI-2” 4-lane interface can be up to 1.5Gbps.

Schematic Notice: Camera (3/10)

- MT6755 image sensor interfaces – MIPI “CSI-2” (2/2)
  - MIPI “CSI-2” 2-lane interface for front-facing camera (sub camera)
    - Differential pair of MIPI CSI, 2-lane:
      - RCP_A/RCN_A
      - RDP0_A/RDN0_A
      - RDP1_A/RDN1_A



    - The data lane number of MIPI CSI can be 1, 2 or 4 lanes.
      - Signals for 1 data lane: {RCP_A / RCN_A } ; {RDP0_A / RDN0_A }
      - Signals for 2 data lane: {RCP_A / RCN_A } ; {RDP0_A / RDN0_A } ; {RDP1_A/ RDN1_A }
      - Signals for 4 data lane: {RCP_A / RCN_A } ; {RDP0_A / RDN0_A } ; {RDP1_A / RDN1_A } {RDP2_A / RDN2_A } ; {RDP3_A / RDN3_A }
    - The MIPI CSI 2-lane interface is pin-multiplexed with serial interface (CM).
    - The data receiving throughput of MIPI CSI 2-lane interface can be up to 1.5Gbps.
    - If MIPI CSI0/CSI1 function is used, the unused pins can not be used as GPI

Schematic Notice: Camera (4/10)

- MT6755 image sensor interfaces – Serial 4-bit (1/2)
  - Serial interface (CM) is pin multiplexed with MIPI CSI sub 2-lane
    - CM signals
      - CMMCLK (MCLK)
      - CMCSK (PCLK)
      - CMCSD[0:3] (4-bit data)
      - I2C-1

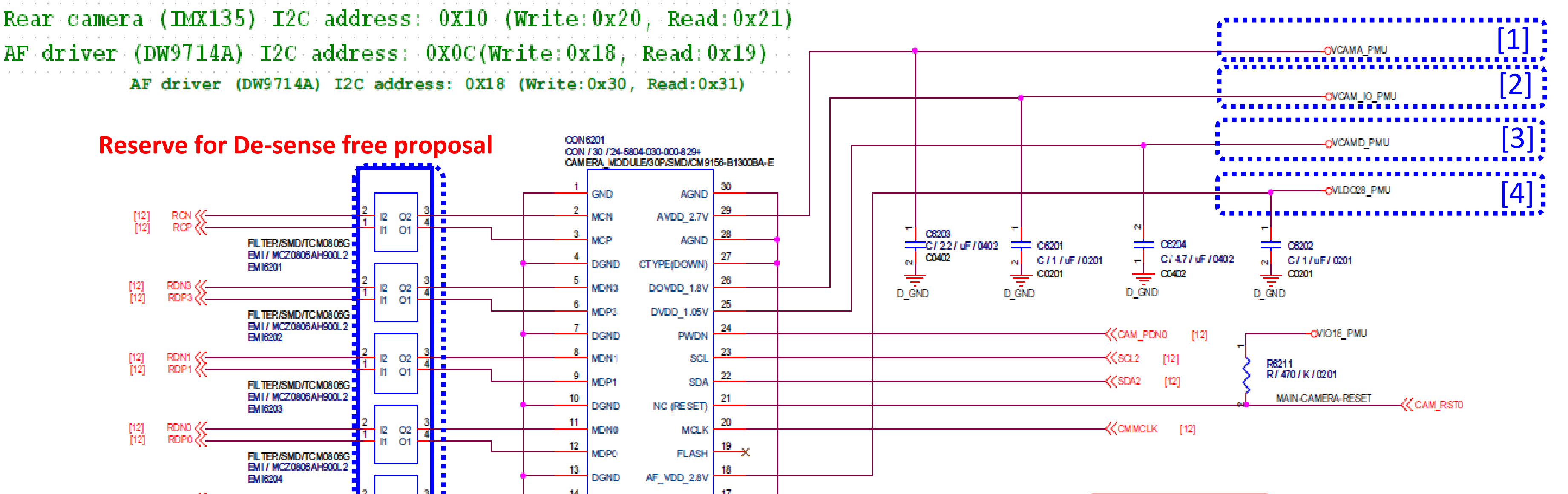
BGA NetName		Aux Func.0	Aux Func.1	Aux Func.2
RDN0_A		GPI	x I:RDN0_A	I0*CMCSD2
RDP0_A		GPI	x I:RDP0_A	I0*CMCSD3
RDN1_A		GPI	x I:RDN1_A	I0*CMCSK
RDP1_A		GPI	x I:RDP1_A	
RCN_A		GPI	x I:RCN_A	I0*CMCSD0
RCP_A		GPI	x I:RCP_A	I0*CMCSD1

    - Supports 0.3M
    - IO level is defined by “DVDD18_VIO”.
    - MIPI CSI-2 is not supported when SPI interface is enabled.

Schematic Notice: Camera (5/10)

- Application circuit of rear facing camera
  - Power supply (1/2)
    - Analog 2.8V power of camera module is powered by PMU's VCAM_A. [1]
    - I/O 1.8V power of camera module is powered by PMU's VCAM_IO. [2]
    - Core power of camera module is powered by PMU's VCAMD_PMU. [3]
    - Auto focus (AF) 3.3V power of camera module is powered by PMU's VLDO28_PMU. [4]

    Note: Core power of camera module can also powered by external LDO, depending on power domain.



ALDO	VCAMA	VBAT_LDOS1	2.8	Off	300mA	2.2uF±20%	6.9uF±20%
SLDO	VCAMIO	AVDD20_SLDO1	1.8	Off	200mA	1uF±20%	3uF±20%
SLDO	VCAMD	AVDD14_SLDO2	0.9/1.0/1.05/1.1/1.21	Off	1200mA	4.7uF±20%	6.9uF±20%

Note: Check the voltage/current requirement of your selected camera sensor and compare them with the relevant spec of their power source.

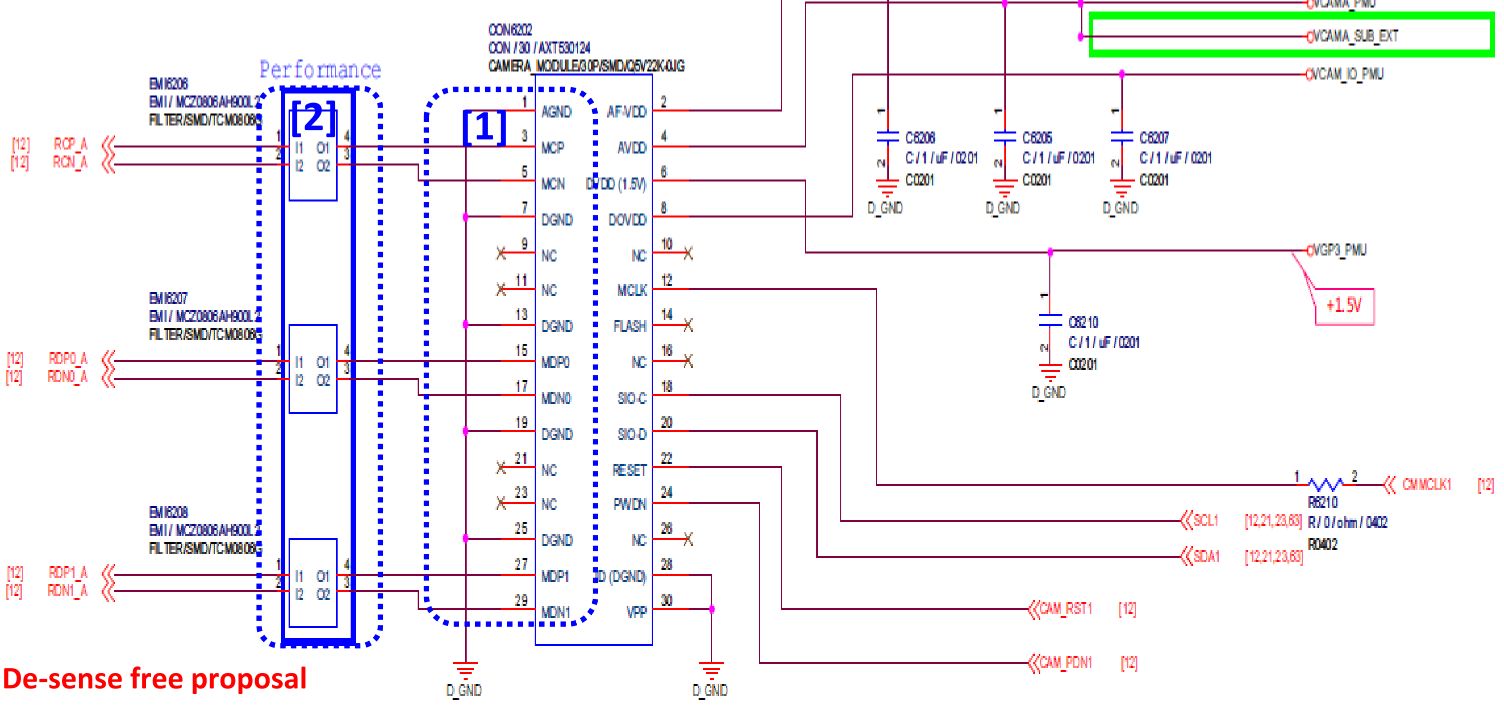
Schematic Notice: Camera (6/10)

- Application circuit of front facing camera
  - MIPI CSI interface
    - We suggest you insert a ground (G) signal between differential pairs to improve inter-lane cross coupling. [1]
    - We suggest you reserve common-mode choke to prevent RF de-sense. The max. cap loading of common-mode choke should be less than 3pF. [2]

Front Camera

Front camera (OV5648) I2C address: 0X36 (Write:0x6C, Read:0x6D)

AF driver (AD5820) I2C address: 0X0C (Write:0x18, Read:0x19)



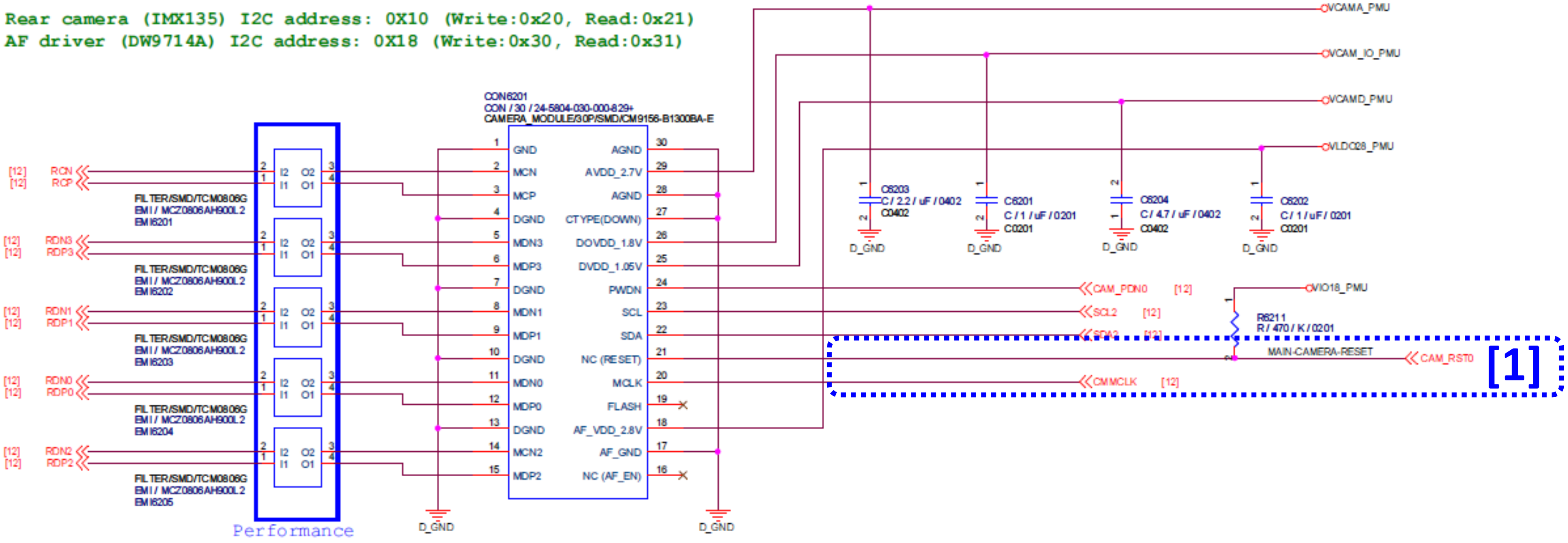
Reserve for De-sense free proposal

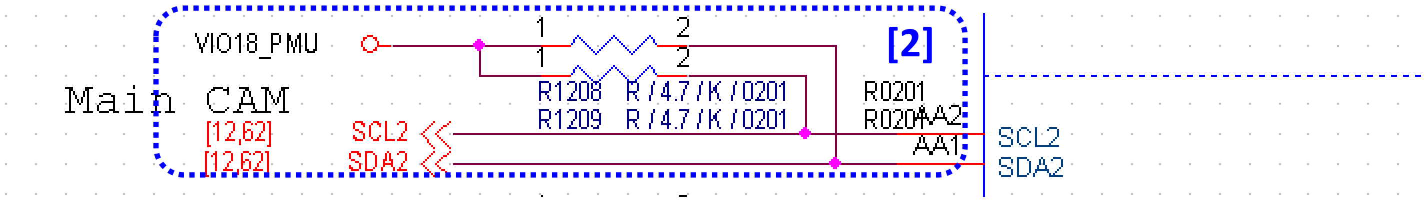
Schematic Notice: Camera (7/10)

- Application circuit of rear facing camera
  - I2C/SCCB control interface
    - I2C-2 (SCL2 & SDA2) controls the main-camera sensor module. [1]
    - There should be external pull-up resistors for I2C open-drain I/O. [2]

Rear Camera

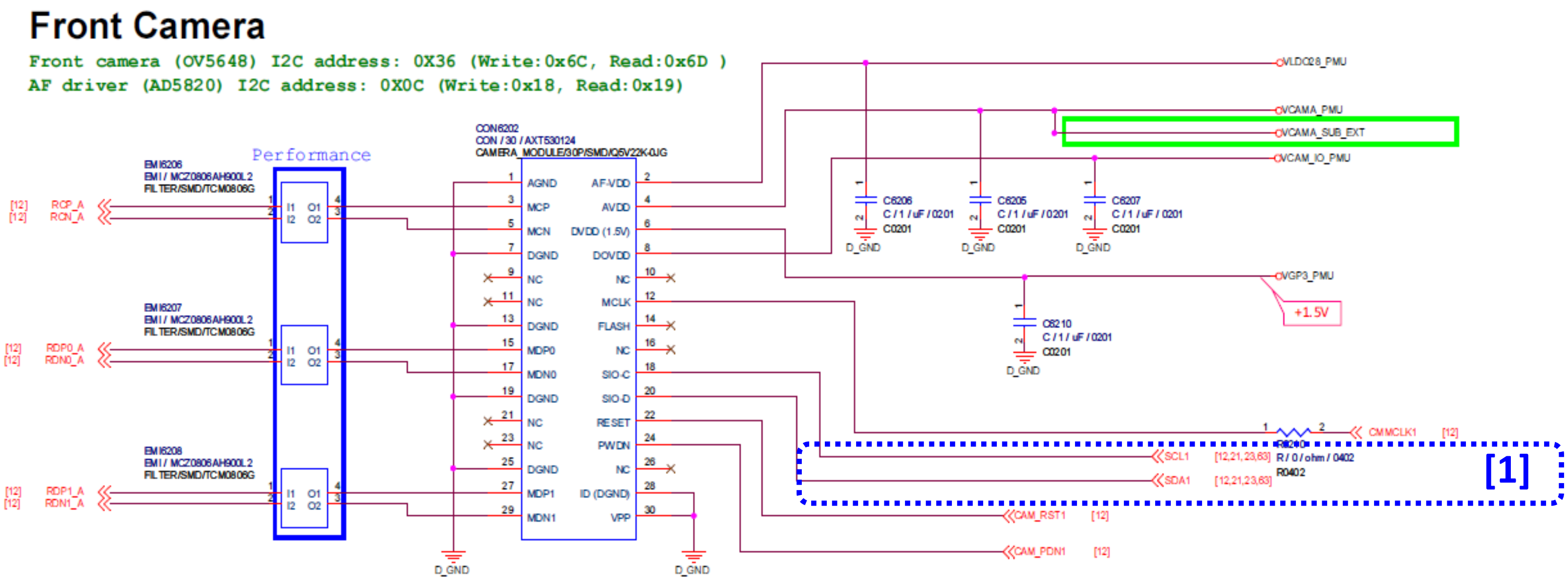
Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21)
AF driver (DW9714A) I2C address: 0X18 (Write:0x30, Read:0x31)

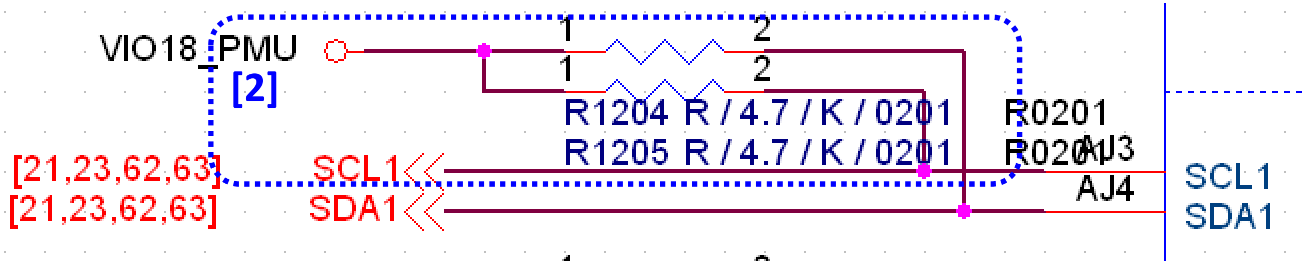




Schematic Notice: Camera (8/10)

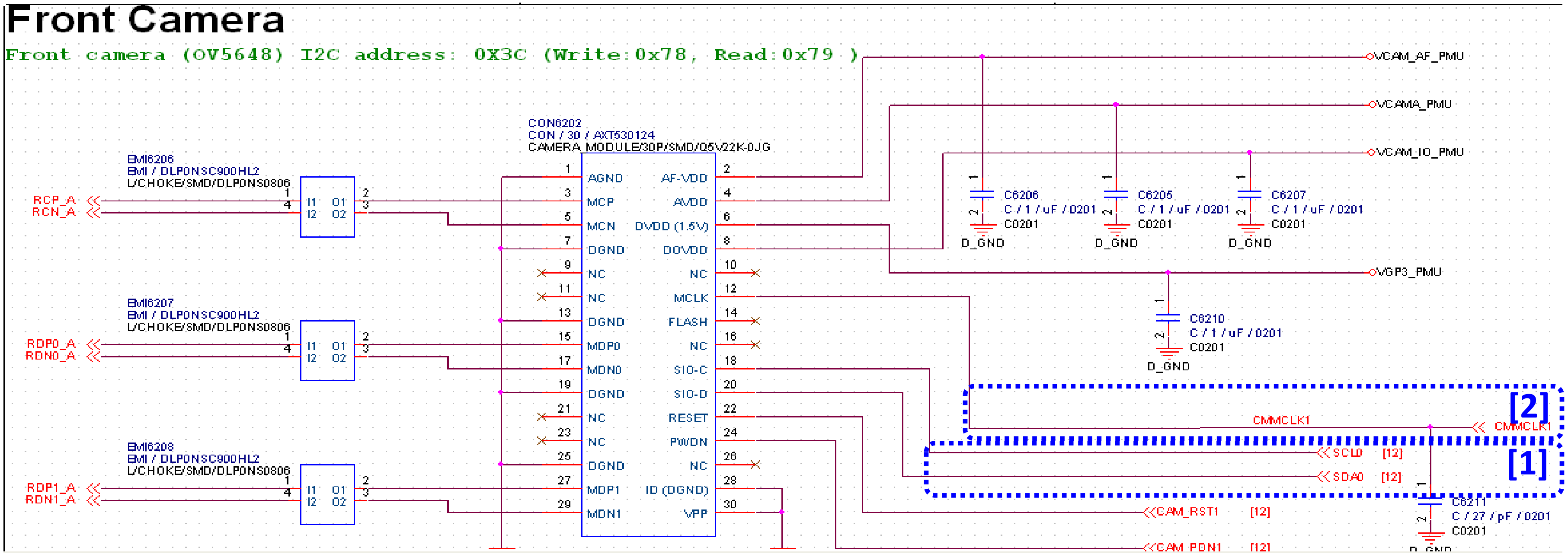
- Application circuit of rear facing camera
  - I2C/SCCB control interface
    - I2C-1 (SCL1 & SDA1) controls sub-camera sensor module. [1]
    - There should be external pull-up resistors for I2C open-drain I/O. [2]





Schematic Notice: Camera (9/10)

- Application circuit of front facing camera
  - I2C/SCCB control interface
    - I2C-2 (SCL2 & SDA2) and I2C-1 (SCL1 & SDA1) control main camera and sub camera respectively. [1]
      If **PIP** (picture in picture) function is supported, using above I2C is recommended since the AF driver I2C address will conflict with the main camera. If the **AF driver is different** in the main and sub camera, using I2C-2 is recommended.
    - GND shielding in **CMMCLK1** is recommended. [2]



MT6755 PIP Feature Design Note

- **Sensor**
  - No additional limitation in camera sensor selection (should also be on MTK DRL)
- **CMMCLK**
  - Separate CMMCLK design
    - Use CMMCLK in main camera and CMMCLK1 in sub camera
- **I2C**
  - Main/sub camera can use the same I2C if AF driver I2C slave address is different.
    - Connecting main/sub camera to I2C2 is suggested.
  - Main/sub camera should use separated I2C if AF driver I2C slave address is the same.
    - Connecting main camera to I2C2 is suggested.
    - Connecting sub camera to I2C1 is suggested.
- **AVDD/DVDD**
  - AVDD of main/sub camera should be separated.
    - Connect main camera to MT6351 VCAMA and sub camera to external LDO.
  - DVDD of main/sub camera should be separated.
    - Connect main camera to MT6351 VCAMD and sub camera to MT6351 VGP3.

MT6755 Camera Capabilities

Application scenario	Rear or front sensor	Interface/Throughput	Sensor resolution @ frame rate per sec.
A	Rear (main)	CSI 4-lane/1.5Gbps	16M@30fps / 21M@15fps
	Front (sub)	CSI 4-lane/1.5Gbps	16M@30fps / 21M@15fps
C	Rear (main)	CSI 4-lane/1.5Gbps	16M@30fps / 21M@15fps
	Front (serial)	Serial	0.3MP@30fps

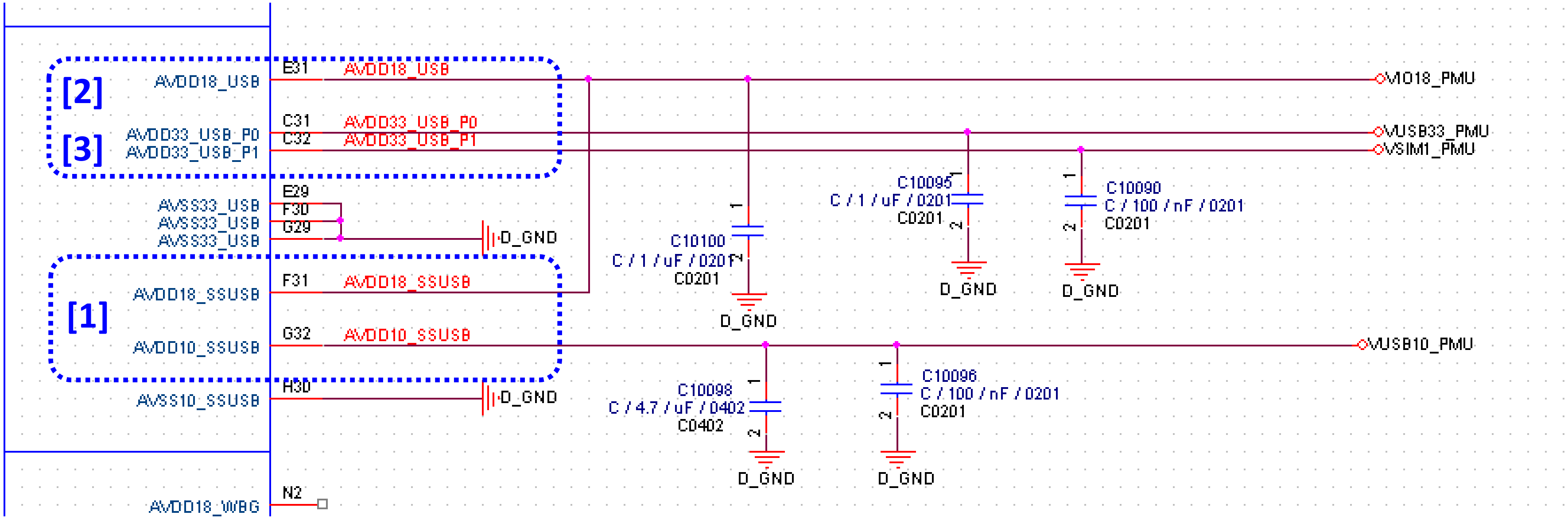
Recommended MIPI application	4+4 lane
Main camera	RCP/RCN RDP0/RDN0 RDP1/RDN1 RDP2/RDN2 RDP3/RDN3
Sub camera	RCP_A/RCN_A RDP0_A/RDN0_A RDP1_A/RDN1_A RDP2_A/RDN2_A RDP3_A/RDN3_A

For more information on camera generic design notice, refer to DCC.

(.. > HW > Common Design Notes > Camera)

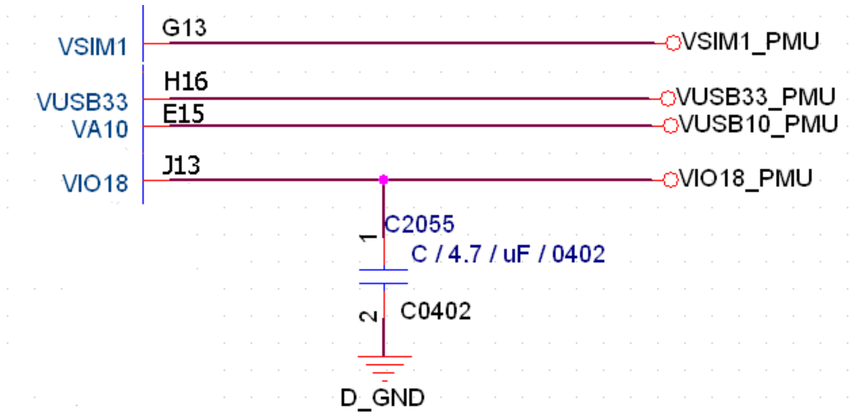
Schematic Notice: USB (1/7)

- MT6755 USB power supply
  - USB power
    - **USB Port 0** (The decouple capacitance should be reserved.)
      - **USB super speed:** AVDD10_SSUSB/AVDD18_SSUSB [1]
        - AVDD10_SSUSB is powered by PMIC VUSB10_PMU; AVDD18_SSUSB is powered by PMIC VIO18_PMU.
      - **USB HS/FS:** AVDD18_USB/AVDD33_USB_P0 [2]
        - AVDD33_USB_P0 is powered by PMIC VUSB33_PMU; AVDD18_USB_P0 is powered by PMIC VIO18_PMU.
    - **USB Port 1** (The decouple capacitance should be reserved.)
      - **IC-USB:** AVDD33_USB_P1 [3]
        - AVDD33_USB_P1 is powered by PMIC **VSIM1_PMU.**



Schematic Notice: USB (2/7)

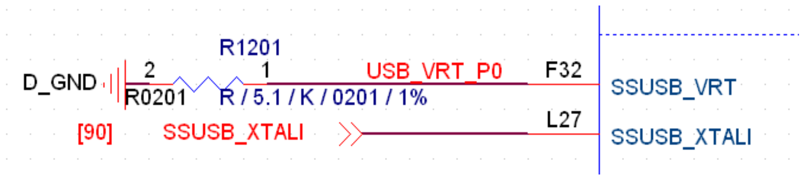
- MT6755 USB power supply
  - USB power
    - **USB Port 1** (The decouple capacitance should be reserved.)
      - **USB HS/FS:** AVDD33_USB_P1
        - AVDD33_USB_P1 is powered by PMIC **VUSB33_PMU.**
      - **Not used:** AVDD33_USB_P1
        - AVDD33_USB_P1 is powered by PMIC **VUSB33_PMU.**
    - Power from PMIC LDO output
      - VIO18_PMU, from MT6351
      - VUSB10_PMU, from MT6351
      - VSIM1_PMU, from MT6351 for IC-USB
      - VUSB33_PMU, from MT6351



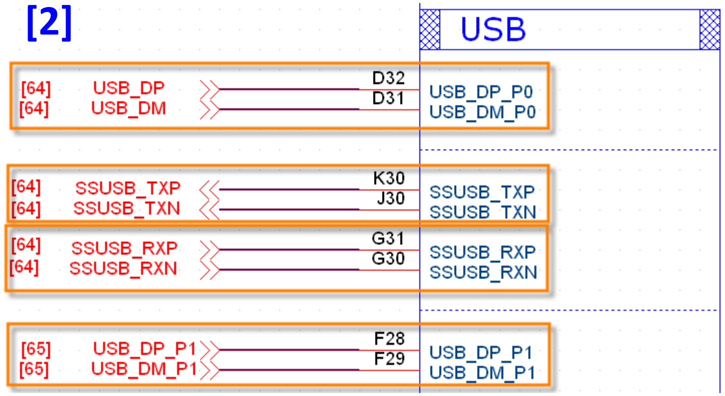
Schematic Notice: USB (3/7)

- MT6755 USB schematic (1/5)
  - SSUSB_VRT: 5.1K reference resistor for USB PHY reference current source. [1]
    - The SSUSB_VRT resistor **should be 5.1K-ohm** and with 1% precision.
    - The SSUSB_USB_VRT resistor should be placed as close to main chip's USB_VRT ball as possible in PCB layout.
    - Be aware of SSUSB_VRT pin; it's trace routing should be away from noise source and high speed clock data like camera data bus.
  - USB differential pair: The **90-ohm** characteristic impedance should be implemented in PCB layout. [2]
    - USB_DM_P0/ USB_DP_P0
    - USB_DM_P1/ USB_DP_P1
    - SSUSB_TXP/SSUSB_TXN
    - SSUSB_RXP/SSUSB_RXN

[1]

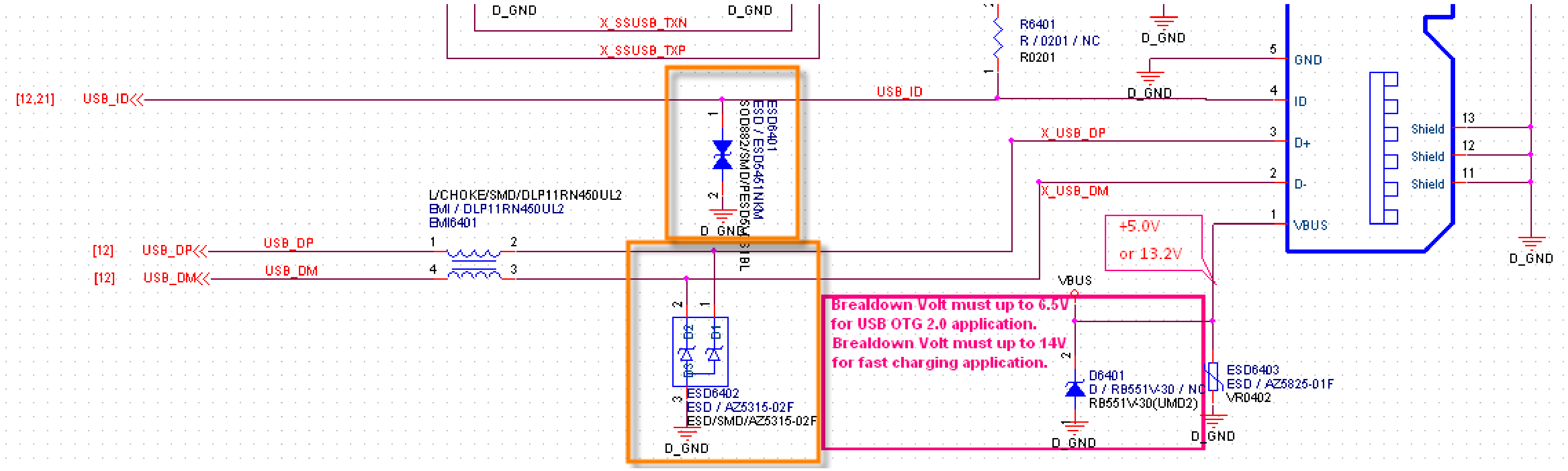


[2]



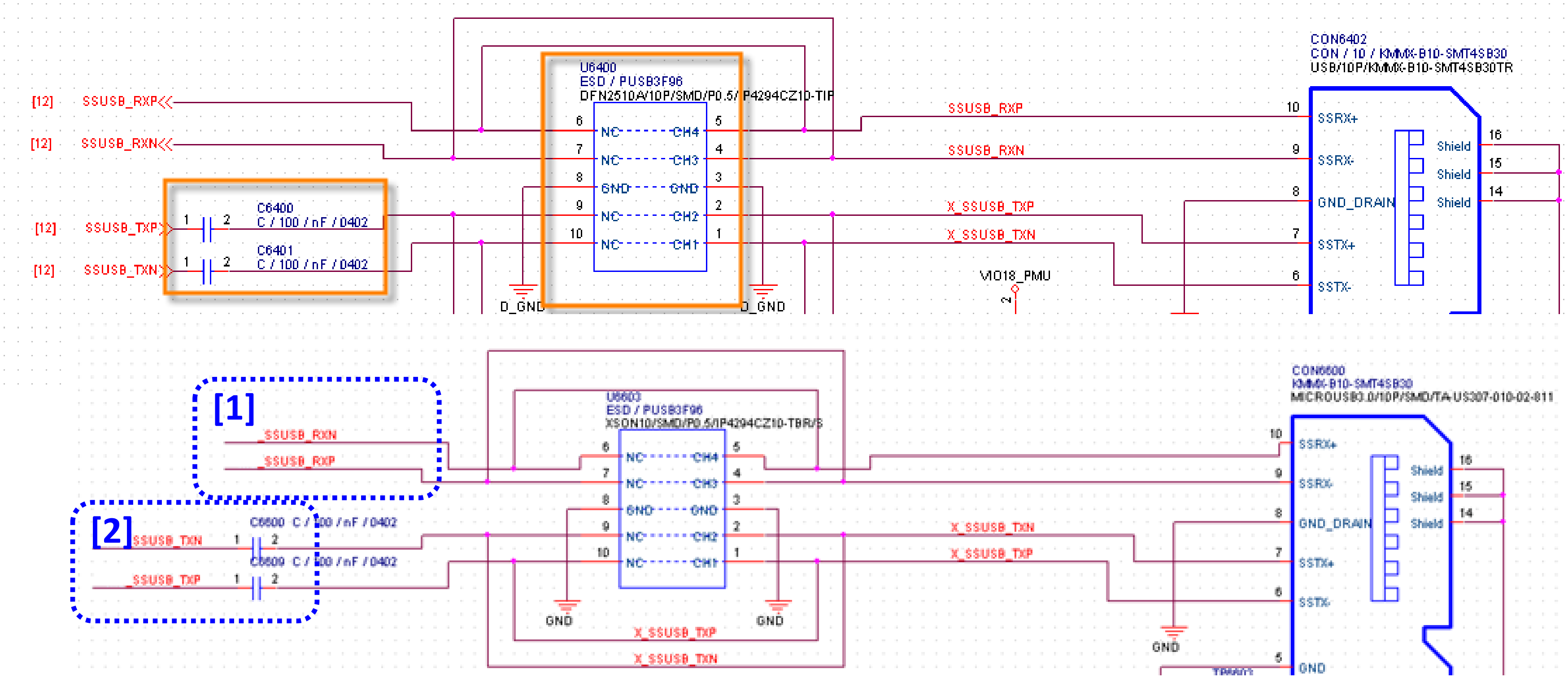
Schematic Notice: USB (4/7)

- MT6755 USB schematic (2/5)
  - USB application circuit on HS/FS receptacle side
    - Reserve ESD protection device for USB differential pair and USB ID pin.
    - The equivalent capacitance loading of ESD protection device should be less than **3pF**.
    - Beware of the diode operate voltage to avoid the leakage current.



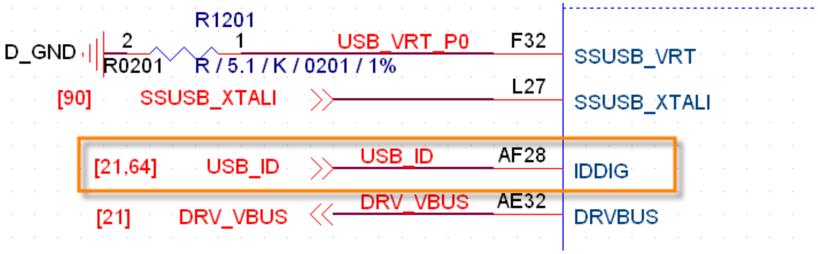
Schematic Notice: USB (5/7)

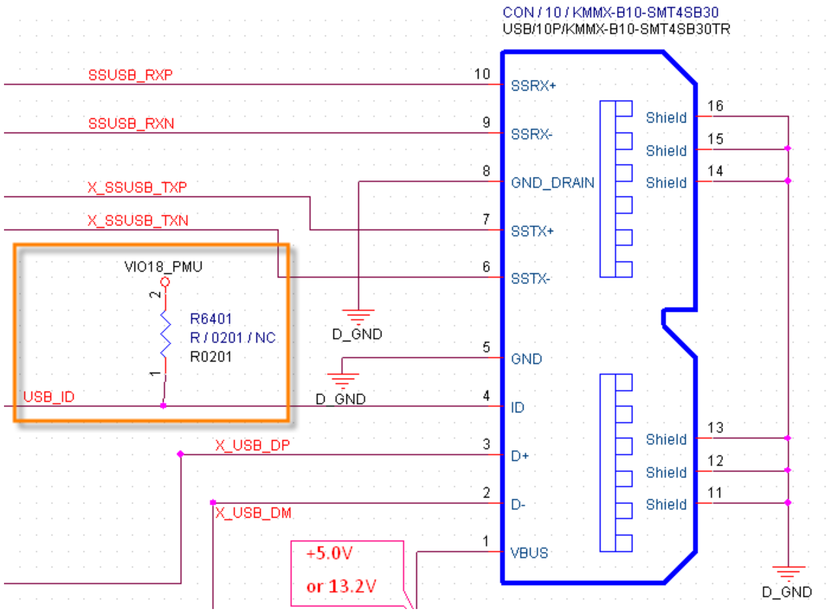
- MT6755 USB schematic (3/5)
  - USB application circuit on super speed receptacle side
    - SSUSB_TXP and SSUSB_TXN **should be** connected to **0.1uF DC blocking** capacitance.
    - Reserve ESD protection device for SSUSB differential pair.
    - The equivalent capacitance loading of ESD protection device should be less than **0.5pF**.
    - The SSUSB_TXP, SSUSB_TXN could swap. [1]
    - The SSUSB_RXP, SSUSB_RXN could swap. [2]



Schematic Notice: USB (6/7)

- MT6755 USB schematic (4/5)
  - USB OTG 2.0 support
    - MT6755 supports full OTG function.
    - IDDIG or IDDIG MUX pin is detected by GPIO, please see the table list below.
    - **Beware of plugging in a MHL cable without build-in MHL switch. (It might damage the ID pin)**



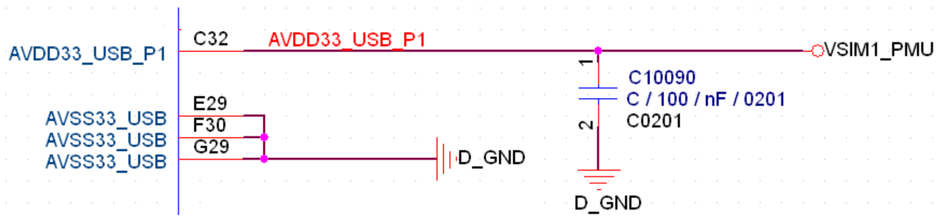


IDDIG	Description
GPIO 0/6/11/23/45/78/116	**Internal Pull up 75k ohm (Recommend to use one of these GPIOs for IDDIG application)**
GPIO 42	**Internal Pull up 200k ohm; For pass OTG2.0, recommend reserve external pull up resistor 75k ohm**

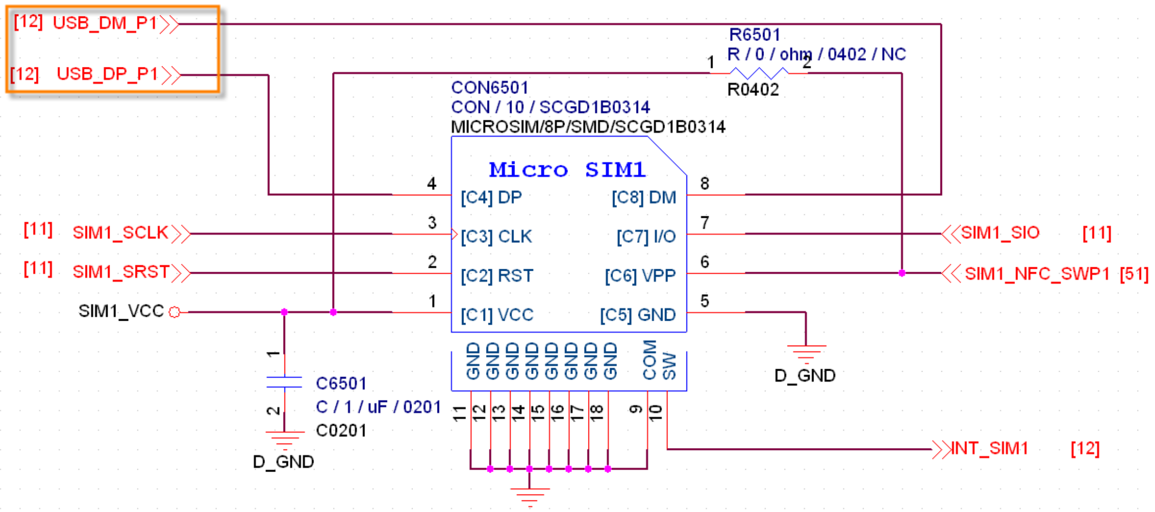
Schematic Notice: USB (7/7)

- MT6755 USB schematic (5/5)
  - IC-USB support
    - MT6755 supports IC-USB (smart card) function.
      - Connect VSIM1_PMU to AVDD33_USB_P1.[1]
      - Connect USB_DP_P1 & USB_DM_P1 to SIM connector.[2]

[1]



[2]



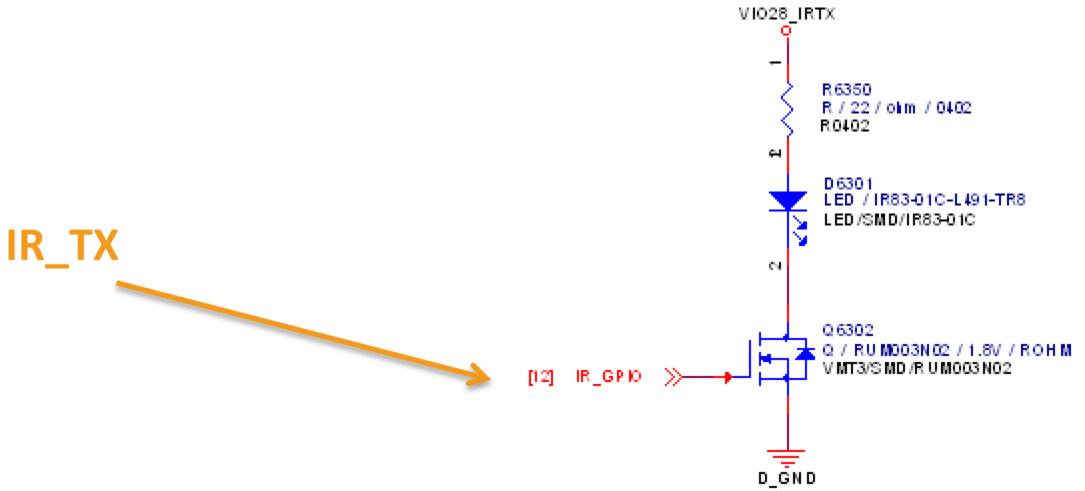
For more information on USB generic design notice, refer to DCC.

(… > HW > Common Design Notes > USB)

Schematic Notice: IR_TX (1/5)

- MT6755 supports IR_TX function.
  - Choose pin mux with O:IRTX_OUT or O:PWM_A/B/C for IR_TX function
  - For PWM_A/B/C, please refer to MT6755_GPIO_Formal_Application_Spec

Pin Name	GPIO reset default mode	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7
EINT6	0	EINT6	**GPIO6**	O:IRTX_OUT	B0:I2S0_LRCK	I1:IDDIG	I1:MD_URXD0	B1:SDA0	O:ANT_SEL5	O*SPI1_B_MO
EINT7	0	EINT7	**GPIO7**	O:IRTX_OUT	I0:I2S0_DI	O:USB_DRVVBUS	O:MD_UTXD0	B1:SCL0	B0:PCC_PPC_IO	O*SPI1_B_CLK
EINT9	0	EINT9	**GPIO9**	O:PWM_B	I1:UCTS1	B1:DAP_SIB1_SWD	O:CONN_MCU_DBGAC	O:IRTX_OUT		B0:DBG_MON_A45
EINT11	0	EINT11	**GPIO11**	O:IRTX_OUT	I1:IDDIG	O*I2S1_MCK	O:PWM_B	O*CLKM0	I0:SRCLKENAI1	
EINT12	0	EINT12	**GPIO12**	O:IRTX_OUT	O:USB_DRVVBUS	I0:I2S2_DI	O:PWM_C	O*CLKM1	O:CMFLASH	
MISC_BSI_DO_3	1	EINT75	GPIO75	**B0*MIPI3_SDATA**	O:PWM_C	O:IRTX_OUT	I0:I2S0_DI	I0:I2S2_DI	O:ANT_SEL5	B0:DBG_MON_B19
MISC_BSI_DO_2	1	EINT77	GPIO77	**B0*MIPI2_SDATA**	O:USB_DRVVBUS	O:IRTX_OUT	B0*I2S0_BCK	O*I2S2_BCK	O:ANT_SEL3	B0:DBG_MON_B21
KPROW1	0	EINT101	**GPIO101**	B1:KPROW1	O:IRTX_OUT	B0:C2K_UTXD1	O:C2K_UTXD0	B0:C2K_DM_EINT2	O:ANT_SEL5	B0:DBG_MON_A36
ANT_SEL0	0	EINT114	**GPIO114**	O:ANT_SEL0	O:PWM_A	O*CLKM0	O:IRTX_OUT	B0:PCC_PPC_IO		B0:DBG_MON_A47
ANT_SEL2	0	EINT116	**GPIO116**	O:ANT_SEL2	O:PWM_C	O*CLKM2	I1:IDDIG	I0:DAP_SIB1_SWCK	O:IRTX_OUT	B0:DBG_MON_A49



Schematic Notice: IR_TX (2/5)

Component choice and IR_TX distance

1. Q6302(MOS)
   - Low on-resistance
   - Low voltage drive (1.8V) makes this device ideal for portable equipment.

2. D6301 (IR_LED)

品名	Dimension(mm)	Wavelength	Intensity	view angle
IR83-01C/L491/TR8	1.6 x 0.8 x 1.52	940nm	4mW/sr at 20mA	X100/Y40deg

3. R6350=22 ohm

Summary	
	Value
R6350	**22ohm**
Q6302(MOS)	**RUM003N02 (1.8V)**
D6301(IR_LED)	**IR83-01C-L491-TR8**
IR TX distance	**> 8.8m (Note 1)**

Note 1: Without lens

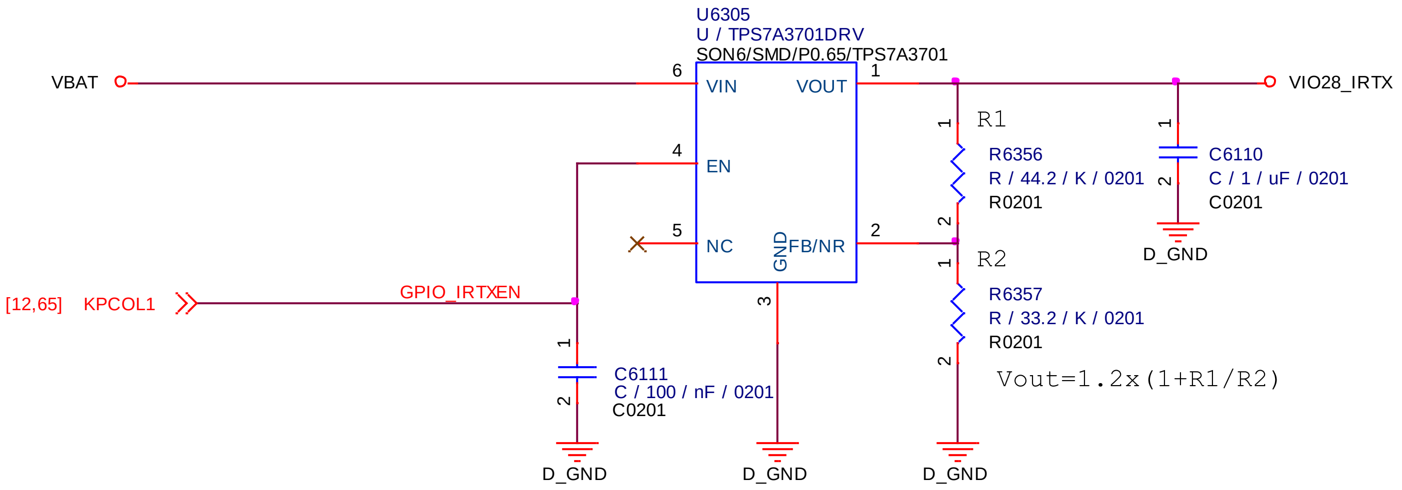
Schematic Notice: IR_TX (3/5)

Choice component and IR_TX distance

4. If customers choose different type of MOS and IR_LED, need to adjust the value of (R6350) resistance to gain the best distance (note2)

Note2:

1. To avoid violating the Absolute Maximum Current Rating of LDO and IR_LED.
2. Typical application circuit for external LDO



Schematic Notice: IR_TX (4/5)

Note2:

3. IR_LED(IR83-01C-L491-TR8) spec

Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Continuous Forward Current	I_F	65	mA
Peak Forward Current *1	I_{FP}	1.0	A
Reverse Voltage	V_R	5	V
Operating Temperature	T_{opr}	-40 ~ +85	℃
Storage Temperature	T_{stg}	-40 ~ +100	℃
Soldering Temperature *2	T_{sol}	260	℃
Power Dissipation at(or below) 25℃ Free Air Temperature	P_d	100	mW

Notes: *1: I_{FP} Conditions--Pulse Width≦100μ s and Duty≦1%.
***2:Soldering time≦5 seconds.**

Schematic Notice: IR_TX (5/5)

Note2:

4. Duty cycle of IR_TX: Default is 33%.
   In this case, the Peak Forward Current of IR_LED(IR83-01C-L491-TR8) should not exceed 300mA.
5. If customers choose different type of IR_LED, need to ask vendor to provide the "peak forward current" for 33% of duty cycle.

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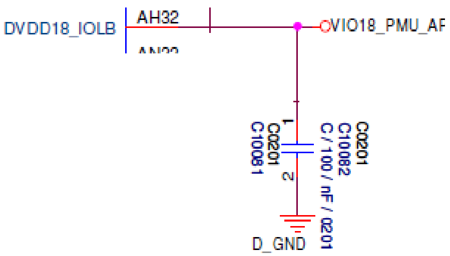
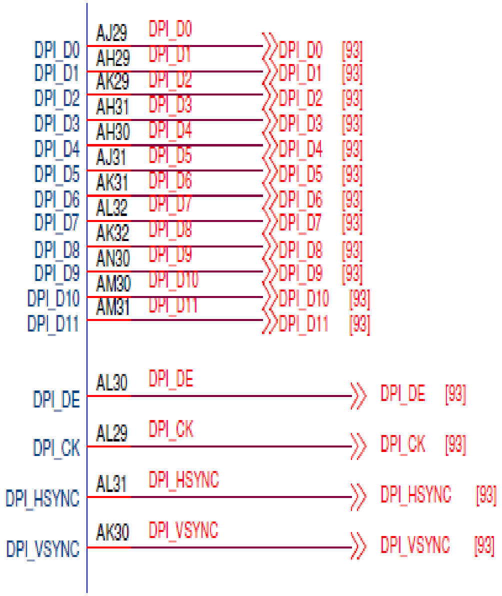
Schematic Notice: DPI (1/3)

- DPI I/O power
  - Power name: “VCC18IO_IOLB”.
    - Reserve a 0.1uF decoupling capacitor on the VCC18IO_IOLB power pad to guarantee PI performance.



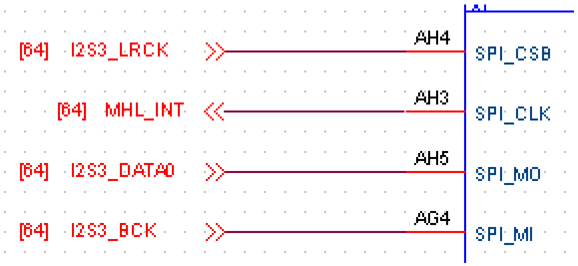
- DPI interface
  - 12-bit DPI data bus: DPI_D[11:0].
  - DPI control interface:
    - DPI_DE
    - DPI_HSYNC
    - DPI_VSYNC
    - DPI_CK (DPI clock)



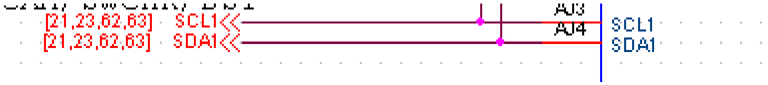
- DPI clock rate
  - The maximum DPI clock frequency can be up to 148.5MHz. Therefore, 2 Trace/1 shielding and keeping reference ground complete are critical in PCB design.

Schematic Notice: DPI (2/3)

- MHL audio interface
  - I2S interface
    - SPI_MI ➔ I2S BCK.
    - SPI_MO ➔ I2S DATA.
    - SPI_CSB ➔ I2S LRCK.



- MHL control interface
  - I2C : I2C1
  - Reset: SPI_CLK
  - INT:



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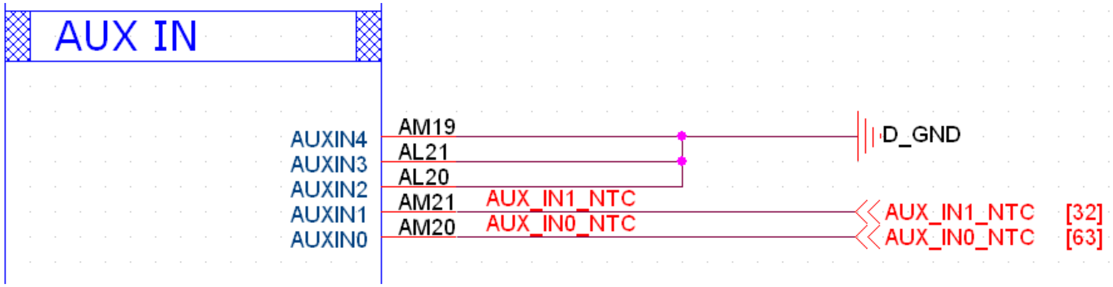
Schematic Notice: DPI (3/3)

- MHL transmitter should be put in the shielding case
- DPI_CK must be shielded by GND.
- Differential 90-ohm characteristic impedance of MHL_D/MHL_DB differential pair should be implemented. MHL_D/MHL_DB differential pair should be routed to surrounding ground plane.
- The DPI signal should be grouped by 2 or 3 and shielded by ground.

Schematic Notice: Auxiliary ADC (1/2)

- **MT6755 has x5 AUXADC channels**
  - 5 auxiliary ADC channels (AUXIN[4:0])
  - Supports max. 1.45V input range
  - 12-bit resolution

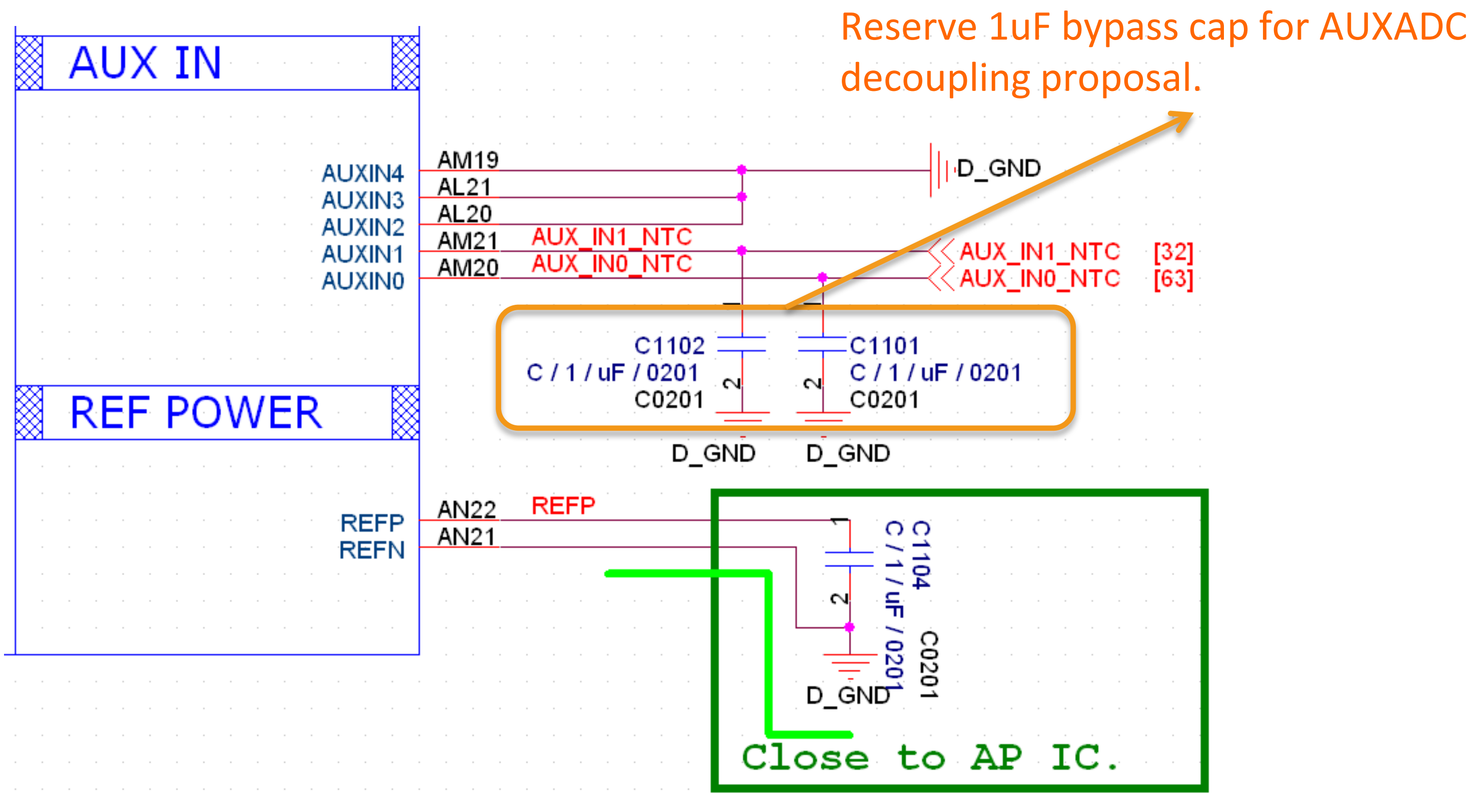
MT6755 ADC	IO power domain	Dedicate pin	Input range	Resolution	Sampling rate
AUXIN0	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	3.25/(N+4) MSPS @ N-bit
AUXIN1	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	
AUXIN2	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	
AUXIN3	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	
AUXIN4	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	



Connect AUXADC to ground when not in use (to avoid de-sense issues)..

Schematic Notice: Auxiliary ADC (2/2)

- **AUXADC needs decouple cap.**
  - Reserve 1uF bypass cap near AP when using the AUX_ADC pin for decoupling RF noise.
  - If all AUX_ADC ports are not used as ADC, you can use all of them as GPI or EINT function; also reserve C0402/C0201 footprint near AP for bypass cap. (Default: NC)

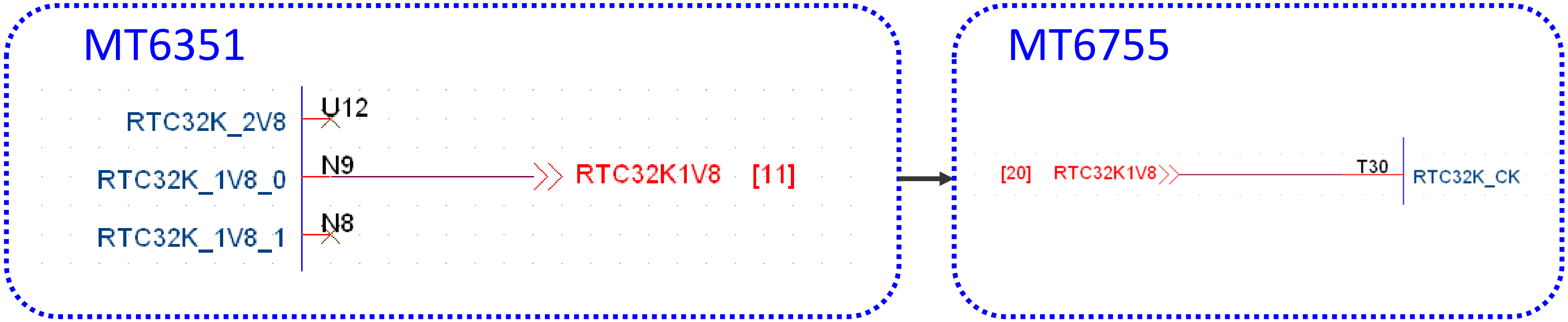


Schematic Notice: Clock Input

- One 26M clock source input to support dual embedded modem.
  - MT6755's clock is DC-coupled input without capacitor in series connection.

Clock source	MT6755 clock input	MT6755 AP	MT6755 MDSYS1	MT6755 MDSYS3
MT6176's XO1 (R1)	MAIN_X26M_IN (AH18)	V	V	V

- "RTC32K_CK" (1.8V) 32kHz input is driven by MT6351's "RTC32K_1V8".



Schematic Notice – PWM

- MT6755 has x3 PWM controller: PWM[A:C]
  - PWM[A:C] @ MT6755 support mode
    - Clock source:

Mode	OLD_MODE	CLKSEL_OLD	CLKSEL	CLKSRC
Old mode	1	Don’t care	0	bclk [1]
Old mode	1	1	1	32KHz (used in old mode only)
Old mode	1	0	1	bclk/1625
FIFO mode	0	Don't care	0	bclk
FIFO mode	0	Don't care	1	bclk/1625
Note 1: The bclk can be selected as 26MHz or 66MHz (bus clock)				

      - Note: bclk can be selected as 26MHz or 66MHz (bus clock) by PWM_CK_26M_SEL.
    - Mode

Mode	Duty cycle	Output frequency
Old mode	PWM_THRESH / (PWM_DATA_WIDTH + 1)	SRCLK / (CLK_DIV * (PWM_DATA_WIDTH + 1))
FIFO mode	Output freq. = (SRCLK * duty cycle) / 4 ; where the unit of duty cycle is % (percentage).	

      - Note: PWM cannot work in sleep mode due to located in the power down domain.

- MT6755 has x1 dedicated CABC PWM controller: DISP_PWM
  - PWM frequency
    - 26M/(PWM_CLKDIV + 1)/1024
    - 104M/(PWM_CLKDIV + 1)/1024
  - PWM duty cycle range: 0% ~ 100%; 1024 steps

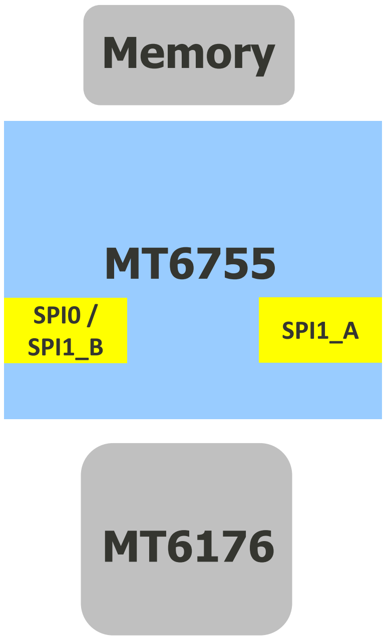
Design Notice: CLKM

- CLKM[0:3] can output clock for external application.
  - Only 32k clock output can exist in suspend mode.
  - If you need 32k clock output in suspend mode, use one of EINT11/EINT12/PWM_A (GPIO11/GPIO12/GPIO100) which guarantees normal 32k output by special IO pad design.
  - See the table below for available clock sources.
  - Supports clock divider (/1, /2, /4, /8, /16… /256) but does not guarantee duty

Clock source of CLKM[0:3]	Note
32kHz	
26MHz	
156MHz	
178.3MHz	
180MHz	

Note: CLK out frequency will not be changed by SSC (spread spectrum clock) or hopping.

Schematic Notice: SPI



- MT6755 supports two HW SPI interfaces.
  - SPI0 is at dedicated SPI pad.
    - SPI0 is default TEE SPI for fingerprint sensor security application
  - SPI1 is PinMux at *SPI1_A (GPIO[25:28])* or *SPI1_B (GPIO[4:7])*
    - Selected by layout direction of application device
    - SPI1 not support TEE SPI for security application
  - Max. data rate: 54Mbit/s
  - Both TX/RX support DMA mode.

Pin Name	GPIO reset default mode	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7
EINT3	0	EINT3	**GPIO3**	O:PWM_A	I1:URXD1	O*CLKM3	O:MD_UTXD2	B1:C2K_URXD1	O:I2S3_DO	I*SPI1_B_MI
EINT4	0	EINT4	**GPIO4**	O:PWM_B	O*I2S0_MCK	I1:UCTS0	I1:MD_URXD1	O:C2K_UTXD0	O:ANT_SEL3	I*SPI1_B_MI
EINT5	0	EINT5	**GPIO5**	O:PWM_C	B0*I2S0_BCK	O:URTS0	O:MD_UTXD1	I1:C2K_URXD0	O:ANT_SEL4	O*SPI1_B_CSB
EINT6	0	EINT6	**GPIO6**	O:IRTX_OUT	B0:I2S0_LRCK	I1:IDDIG	I1:MD_URXD0	B1:SDA0	O:ANT_SEL5	O*SPI1_B_MO
EINT7	0	EINT7	**GPIO7**	O:IRTX_OUT	I0:I2S0_DI	O:USB_DRVVBUS	O:MD_UTXD0	B1:SCL0	B0:PCC_PPC_IO	O*SPI1_B_CLK
DPI_D11	0	EINT24	**GPIO24**	O*DPI_D11	O:USB_DRVVBUS	I0:CONN_DSP_JCK	I*SPI1_A_MI	O:PWM_C	I0:I2S2_DI	B0:DBG_MON_A30
DPI_HSYNC	0	EINT25	**GPIO25**	O*DPI_HSYNC	I*SPI1_A_MI	I1:CONN_DSP_JMS	O*CLKM0	B0:C2K_UTXD1	O*I2S3_MCK	B0:DBG_MON_A31
DPI_VSYNC	0	EINT26	**GPIO26**	O*DPI_VSYNC	O*SPI1_A_CSB	I0:CONN_DSP_JDI	O*CLKM1	B1:C2K_URXD1	O*I2S3_BCK	B0:DBG_MON_A32
DPI_DE	0	EINT27	**GPIO27**	O*DPI_DE	O*SPI1_A_MO	O:CONN_DSP_JDO	O*CLKM2	B0:C2K_DM_EINT2	O:I2S3_LRCK	B0:DBG_MON_A33
DPI_CK	0	EINT28	**GPIO28**	O*DPI_CK	O*SPI1_A_CLK	O:CONN_DSP_JINTP	O*CLKM3	B0:C2K_DM_EINT3	O:I2S3_DO	B0:DBG_MON_A34
SPI_MI	0	EINT95	**GPIO95**	I*SPI0_MI	O:MRG_SYNC	O:PCM0_SYNC	O*I2S1_BCK	O*SPI0_MO	O:DFD_TDO	O:JTDO_SEL1
SPI_CSB	0	EINT96	**GPIO96**	O*SPI0_CSB	O:MRG_DO	O:PCM0_DO	O:I2S1_LRCK	B1:SDA2	I0:DFD_TMS	B1:JTMS_SEL1
SPI_MO	0	EINT97	**GPIO97**	O*SPI0_MO	O*MRG_CLK	O*PCM0_CLK	O:I2S1_DO	I*SPI0_MI	I0:DFD_TDI	I1:JTDI_SEL1
SPI_CLK	0	EINT98	**GPIO98**	O*SPI0_CLK	I:MRG_DI	I0:PCM0_DI	O*I2S1_MCK	B1:SCL2	I0*DFD_TCK_XI	I0*JTCK_SEL1
SRCLKENAI	0	EINT99	**GPIO99**	I0:SRCLKENAI0	O:UTXD1	I0:EXT_FRAME_SYNC	O*CLKM2	B0:PCC_PPC_IO	O:ANT_SEL3	I*SPI0_MI

Schematic Notice: Debug

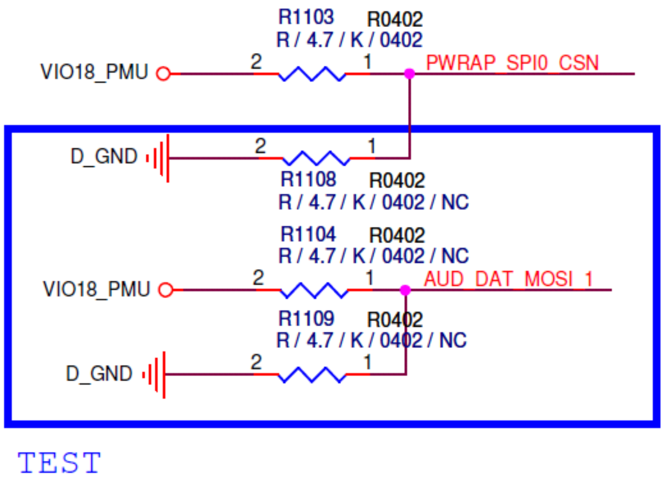
- Debug interface
  - Legacy JTAG (reserve TCK and TMS for serial JTAG)
  - AP UART
  - MD UART[0:2] (PinMux)
  - C2K UART[0:1] (PinMux)

Interface	AP	MD1 (L/W/T/G)	MD3 (C2K)
Legacy parallel JTAG	V	V	V
Serial JTAG	V	V	V
AP UART (UART0)	V		
MD UART[0:2] (pin mux)		V	
C2K UART[0:1] (pin mux)			V

Schematic Notice: JTAG Trapping Table

- JTAG trapping pin
  - PWRAP_SPI0_CSN, MT6755 default PU but MT6351 default PD ➔ Need to add external 4.7k pull-up resistor
  - AUD_DAT_MOSI, default PD
- PinMux function

PWRAP_SPI0_CSN	AUD_DAT_MOSI	JTAG
HI	LO	N/A
HI	HI	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI
LO	LO	CAM_CLK0/CAM_RST0/CAM_RST1/CAM_PDN0
LO	HI	MSDC1_CLK/MSDC1_CMD/MSDC1_DAT0/MSDC1_DAT1



Schematic Notice: Suggestion for RF Assignment

- Refer to MT6755 (BB)/MT6351 (PMIC)’s Connection for MT6176 section in MT6176 design notice.

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